HK32M050 Datasheet

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Preface

Purpose

This document introduces the block diagram, memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32M050 series microcontrollers (MCUs). It helps you quickly understand the characteristics and functions of HK32M050.

Audience

This document is intended for:

- HK32M050 developers
- HK32M050 testers
- HK32M050 users

Release Notes

This document is applicable to HK32M050 series MCUs.

Revision History

Version	Date	Description
1.0	2023/08/04	The initial release.
1.1	2024/01/22	1. Changed the maximum operating frequency in section "2 Product overview" to 64 MHz. 2. Updated the ADC clock frequency and conversion frequency in section "3.15 ADC". 3. Updated section "4.2.15 DAC voltage divider characteristics". 4. Deleted the input bias current from Table 4-24 OPAMP characteristics. 5. Added the description that the TX and RX pin functions of UART can be exchanged to section "6.8 Alternate function table".

Contents

1 Introduction

This document is the datasheet for HK32M050 series MCUs. HK32M050 is a family of MCUs developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd. (hereinafter referred to as Hangshun) specifically for motors. This MCU family includes:

- HK32M050G4U7 (QFN28 package)
- HK32M050G4P7 (TSSOP28 package)
- HK32M050E4U7 (QFN24 package)
- HK32M050E4P7 (TSSOP24 package)
- HK32M050F4U7 (QFN20 package)
- HK32M050F4P7 (TSSOP20 package)

For more details of HK32M050, see *HK32M050 User Manual*.

2 Product overview

HK32M050 is a family of MCUs developed specifically for motors. It adopts the ARM® Cortex®-M0 core and incorporates the patented electric motor acceleration (EMACC) unit of Hangshun. The maximum operating frequency of HK32M050 can reach 64 MHz. Each HK32M050 MCU has 16 Kbytes of Flash and four Kbytes of SRAM.

HK32M050 embeds a 16-bit advanced timer (three PWM output channels in total, which all have complementary PWM outputs with programmable inserted dead-times), a 32-bit general-purpose timer, a 16-bit general-purpose timer, and a 16-bit basic timer.

The analog circuitry embedded in HK32M050 includes a 12-bit ADC (up to six external channels), two operational amplifiers (OPAMPs) that can operate in PGA mode, a voltage comparator (comparator threshold output from DAC), a power-on reset (POR)/power-down reset (PDR)/brown-out reset (BOR) circuitry, and an internal reference voltage (sampled by internal ADC).

Except for the power pins, ground pins, and NRST pin, all the other pins of HK32M050 can be used as GPIOs, peripheral I/Os, or external interrupt inputs. This way, more pin functions can be provided.

HK32M050 supports the conventional Flash read/write protection and also offers the patented Flash code encryption function of Hangshun.

HK32M050 incorporates several communication interfaces: a UART interface, a high-speed SPI, and an I2C interface.

HK32M050 also integrates the division and square root (DVSQ) calculation unit which provides higher performance than software and faster responses to external events.

HK32M050 provides Sleep and Stop low-power modes that can meet the requirements of power consumption-sensitive applications.

With the diversified peripherals, HK32M050 is best suited for the square wave control and field-oriented control (FOC) of brushless direct current (BLDC) motor and permanent magnet synchronous motor (PMSM).

- Electric tools
- Industrial fans
- Compressors
- Electric vehicles
- Range hoods
- Vacuum cleaners
- Water pumps
- Ceiling fans
- Air conditioners

2.1 Feature

- CPU core
  - ARM® Cortex®-M0
  - Maximum frequency: 64 MHz
  - 24-bit SysTick timer
- Operating voltage range
  - Single power domain (V_{DD}): 2.5 V to 5.5 V

- Operating temperature range: –40°C to 105°C
- Typical operating current
  - Run mode
    - 2.88 mA@5 V@8 MHz
    - 6.96 Ma@5 V@64 MHz
  - Sleep mode
    - 0.4 mA@5 V@40 kHz
    - 1.48 mA@5 V@8 MHz
    - 4.4 mA@5 V@64 MHz
  - Stop mode
    - LDO in normal mode: 0.37 mA@5 V@40 kHz
    - LDO in low-power mode: 11.3 µA@5 V@40 kHz
- Memory
  - 16-Kbyte Flash
    - No wait states to access Flash when the CPU frequency is 21 MHz or lower
    - Separate read and write protection for Flash data
    - Encryption for instructions and data stored in the Flash, preventing the damage caused by physical attacks
  - 4-Kbyte SRAM
- Clock
  - High-speed internal clock (HSI): 8 MHz/16 MHz/64 MHz
  - Low-speed internal clock (LSI): 40 kHz
  - GPIO external input clock: 5 MHz to 30 MHz
- Reset
  - External pin reset (NRST pin)
  - Option byte loading (OBL) reset
  - Window watchdog counting terminates (WWDG reset)
  - Independent watchdog counting terminates (IWDG reset)
  - Power reset (POR/PDR/BOR)
  - Software reset (SW Reset)
  - Low-power management reset
- GPIO
  - Provides up to 25 GPIOs
- Data communication interfaces
  - 1 × UART
  - 1 × I2C
    - Transmission rate at 1 Mbit/s, 400 kbit/s, 100 kbit/s
    - Wakes up the MCU from Stop mode when receiving data
  - 1 × high-speed SPI

- Transmission rate at up to 18 Mbit/s

- Timer
  - 1 × 16-bit advanced timer: TIM1
    - Three complementary PWM outputs with programmable inserted dead-times
    - Supports the break function triggered by signals output from external pins or internal comparators
    - The outputs of CC4 to CC6 can trigger ADC at multiple points in time.
  - 2 × general-purpose timers
    - 1 × 32-bit general-purpose timer: TIM2
    - 1 × 16-bit general-purpose timer: TIM3
  - 1 × 16-bit basic timer: TIM6
- Division and square root (DVSQ) calculation unit
  - Supports 32-bit fixed point division, with the quotient and remainder calculated
  - Supports 32-bit fixed point high-precision root calculation
- Electric motor acceleration (EMACC)
  - Supports the coordinate rotation digital computer (CORDIC) algorithm for sine and cosine
  - Supports Clarke, Park, and Inverse Park transformations
  - Supports space vector pulse width modulation (SVPWM)
  - Supports 1 × high-speed motor data transmission channel (Trace)
- On-chip analog circuitry
  - 1 × successive approximation (SAR) ADC
    - 12-bit resolution
    - Maximum conversion frequency: 1.14 MSPS
    - Up to six external analog signal input channels
    - Supports the conversion by four independent regular queues
    - Supports automatic continuous conversion and scan conversion
    - In regular queues, the conversion request of a channel can be redirected to another channel
    - Supports multiple hardware trigger sources (such as TIM1_TRGO, TIM1_CCx, and GPIO input events)
    - Independent register for each channel to save data
  - Internal reference voltage
    - The output of the internal reference voltage is connected to an independent ADC channel.
  - 1 × voltage comparator (COMP)
    - The reference voltage of the comparator is from the external signal input or internal 8-bit DAC.
    - The output of comparators can be used as the break of the advanced timer.
  - 2 × operational amplifiers (OPAMPs)
    - Programmable amplification factor
    - The output signal of amplifiers can be output to pins or an ADC sampling channel.
- 96-bit unique ID (UID) of each MCU
  - Used as the serial number and security key

- Used to activate the secure boot process

- CPU trace and debug
  - SWD debug interface
  - ARM® CoreSight™ debug component (ROM-Table, DWT, BPU)
  - Customized DBGMCU debug controller (for low-power mode simulation control, debugged peripheral clock control, and debug and trace interfaces allocation)
- Reliability
  - Passes HBM6000V/CDM2000V/LU800mA level tests.

2.2 Device overview

Table 2-1 HK32M050 series features

Feature		HK32M050G4U7	HK32M050G4P7	HK32M050E4U7	HK32M050E4P7	HK32M050F4U7	HK32M050F4P7
GPIO		25	25	22	22	18	18
Package		QFN28	TSSOP28	QFN24	TSSOP24	QFN20	TSSOP20
Operating voltage		2.5 V – 5.5 V					
Operating temperature		–40°C to +105°C					
Memory	Flash (Kbyte)	16					
	SRAM (Kbyte)	4					
CPU	Core	Cortex®-M0					
	Frequency	64 MHz					
Division and square root (DVSQ) calculation unit		1					
Clock	LSI	40 kHz					
	HSI	8 MHz/16 MHz/64 MHz					
	GPIO input clock	5 MHz – 30 MHz					
Timer	Advanced timer	1 (16-bit): TIM1					
	General-purpose timer	1 (32-bit): TIM2 1 (16-bit): TIM3					
	Basic timer	1 (16-bit): TIM6					
	SysTick	1					
	IWDG	1					
	WWDG	1					
Comm. peripheral	UART	1					
	I2C	1					
	SPI	1					
ADC	ADC (Channels)	1 (6)					
	Reference selection	Internal reference voltage					
	ADC conversion frequency	1.14 MSPS					
	ADC	12-bit					

Feature		HK32M050G4U7	HK32M050G4P7	HK32M050E4U7	HK32M050E4P7	HK32M050F4U7	HK32M050F4P7
	accuracy						
Voltage comparator (COMP)		1					
Operational amplifier (OPAMP)		2					
Electric motor acceleration (EMACC)		1					
96-bit UID		1					

3 Function description

3.1 Block diagram

HK32M050 integrates a Flash memory of 16 Kbytes to store programs and data.

ARM® Cortex®-M0 is a 32-bit RISC processor, which delivers outstanding computational performance and advanced system responses to interrupts. With the ARM® Cortex®-M0 core embedded, the HK32M050 family is compatible with all ARM tools and software.

The following figure shows the block diagram of HK32M050G4U7 as an example:

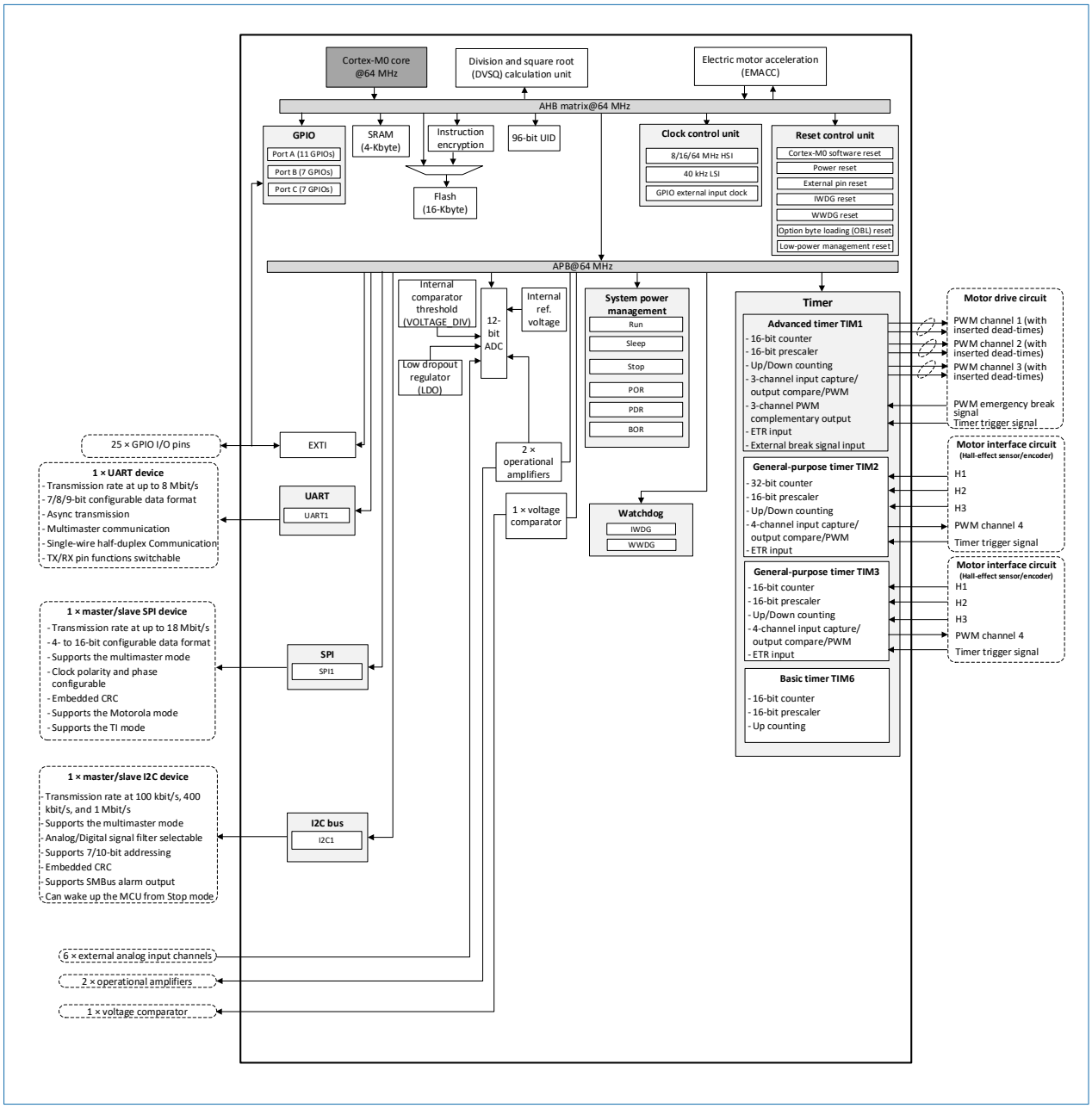

Figure 3-1 HK32M050G4U7 block diagram

3.2 Memory mapping

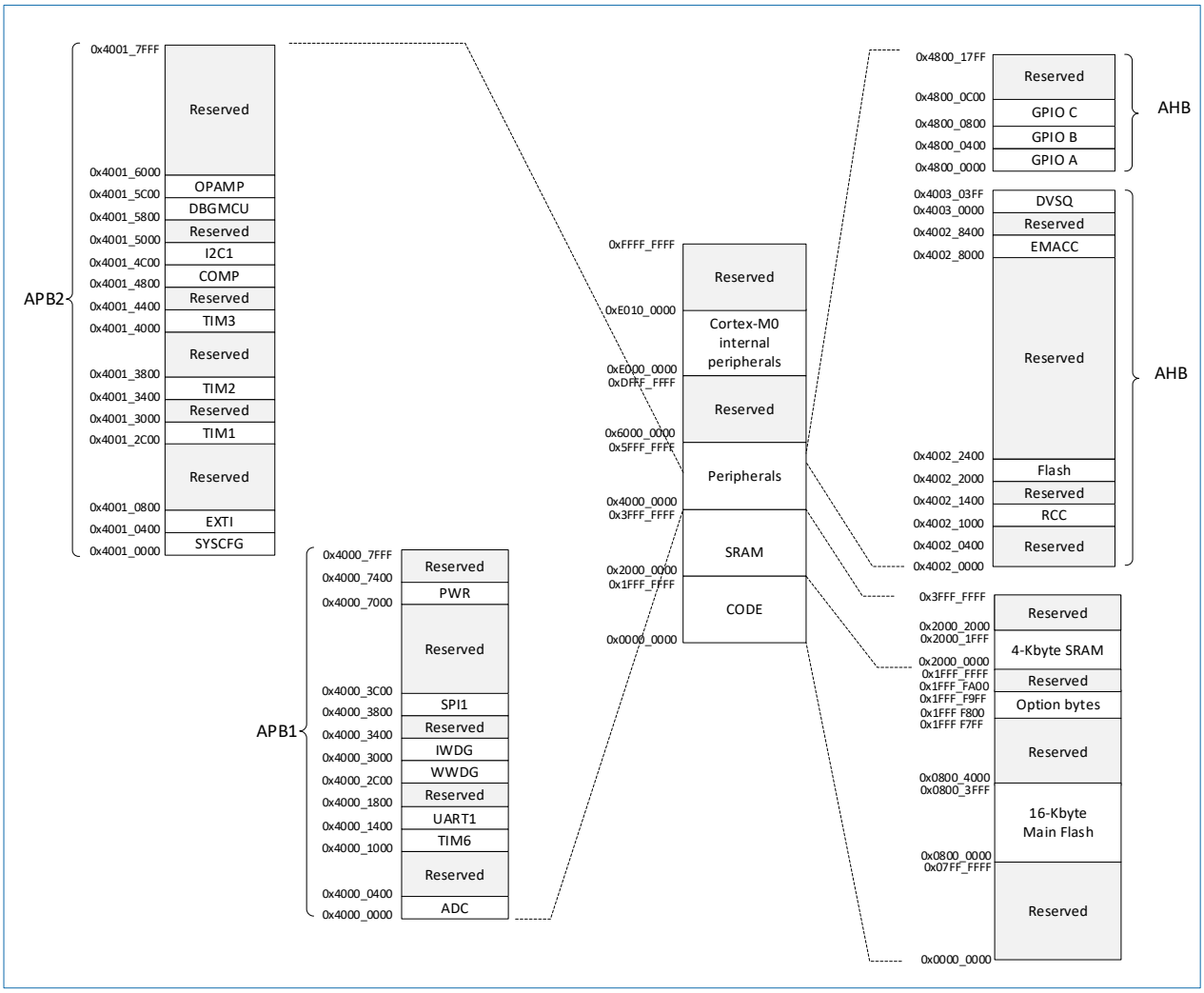

Figure 3-2 HK32M050G4U7 memory mapping

3.3 Memory

3.3.1 Flash

HK32M050 integrates a Flash memory of 16 Kbytes to store programs and data.

3.3.2 SRAM

HK32M050 integrates a 4-Kbyte SRAM which can be accessed in words, half words, or bytes. The CPU can access the SRAM with no wait states, meeting the requirements of most applications.

3.4 Power supply scheme

- V_{DD} = 2.5 V to 5.5 V: The external power supply (no V_{BAT}) supplies power to the digital circuitry, I/O pins, and internal voltage regulator of the MCU.
- V_{DDA} = 2.5 V to 5.5 V: The V_{DDA} pin supplies power to the analog circuitry, such as the ADC, voltage comparator, and operational amplifiers.

  Note: V_{DD} and V_{DDA} are connected internally.

3.5 Power supply monitor

HK32M050 MCUs contain the POR/PDR/BOR circuitry. When the supply voltage reaches 2.5 V, the MCU can work normally. When V_{DD}/V_{DDA} is lower than the specified V_{POR}/V_{PDR} threshold, the MCU will be reset without using

any external reset circuit. During the power-on process, BOR guarantees that the MCU is in the reset state until the supply voltage reaches the specified V_{BOR} threshold. When BOR is disabled, the power supply is under the monitoring of POR/PDR.

3.6 Low-power modes

HK32M050 supports Sleep and Stop low-power modes.

- Sleep mode: Only the CPU stops. All peripherals keep operating. The CPU can be woken up when an interrupt or event occurs.
- Stop mode: MCUs achieve the lowest power consumption while retaining the content in SRAM and registers. In Stop mode, all clocks in the core domain, the PLL, HSI oscillator, and HSE oscillator are disabled. The MCU can be woken up from Stop mode by any extended interrupt/event controller (EXTI) line. The EXTI line source can be any external I/O pin. I2C can wake up the MCU from Stop mode when receiving data.

3.7 Resets

3.7.1 System reset

The system reset resets all registers, except for the reset flags in the control/status register RCC_CSR. You can identify the reset source by checking reset status flags in the RCC_CSR register.

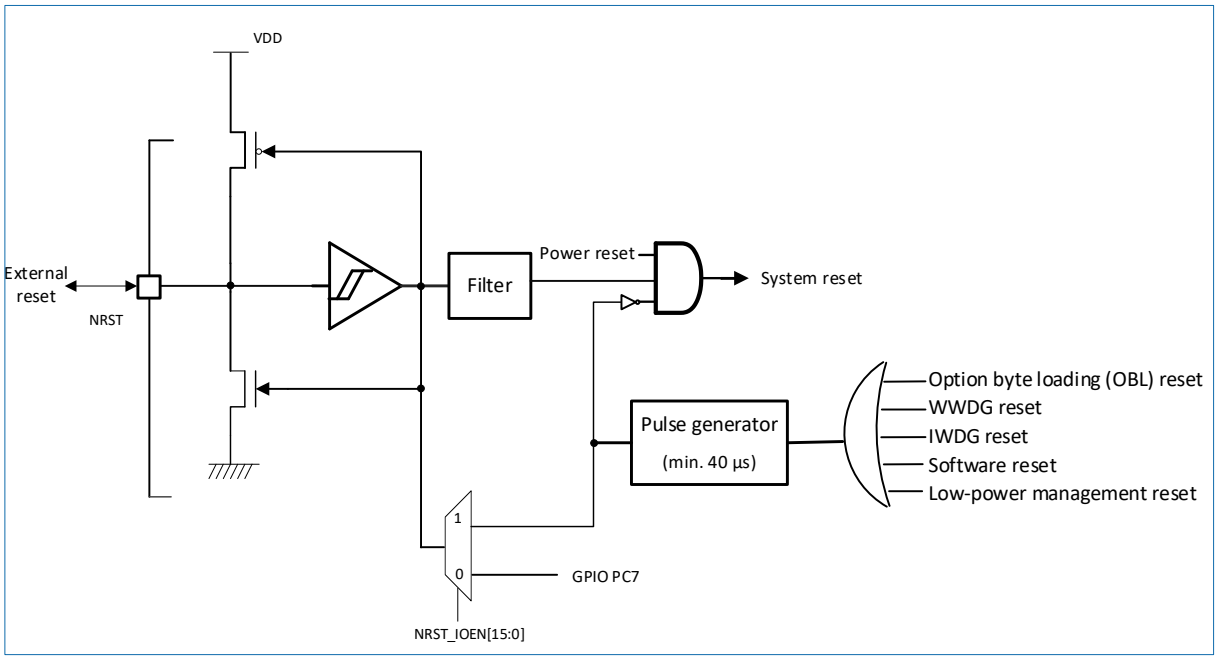

Figure 3-3 Reset signal

A system reset is generated when any of the following events occurs:

- Low level on the NRST pin (external reset)
- Option byte loading (OBL) reset
- Window watchdog counting terminates (WWDG reset)
- Independent watchdog counting terminates (IWDG reset)
- Power reset (POR/PDR/BOR)
- Software reset (SW reset): The SYSRESETREQ bit in Cortex®-M0 Application Interrupt and Reset Control Register must be set to 1 to force a software reset on the device.
- Low-power management reset

Except for the power reset, the reset sources of other resets eventually act on the NRST pin. The NRST pin keeps

the low level during resets. The reset routine vector is fixed at address 0x0000 0004. The internal reset signals (except for the power reset) are output on the NRST pin. The pulse generator guarantees a reset pulse duration of at least 40 µs for each internal reset source. When the NRST pin is pulled low and an external reset is generated, the reset pulse is generated.

3.7.2 Power reset

A power reset is generated when any of the following events occurs:

- Power-on reset (POR)/Power-down reset (PDR)
- Brown-out reset (BOR)

HK32M050 MCUs contain the POR/PDR circuitry. The circuitry keeps operating to ensure that the system runs properly when the power supply exceeds the 2.5 V threshold. When V_{DD} is less than the POR/PDR threshold, the MCU will be reset without using any external reset circuit.

HK32M050 also integrates brown-out reset (BOR). By default, BOR is unavailable. The power supply is under the monitoring of POR/PDR. You can configure the option byte to enable or disable BOR.

3.8 Clocks and clock tree

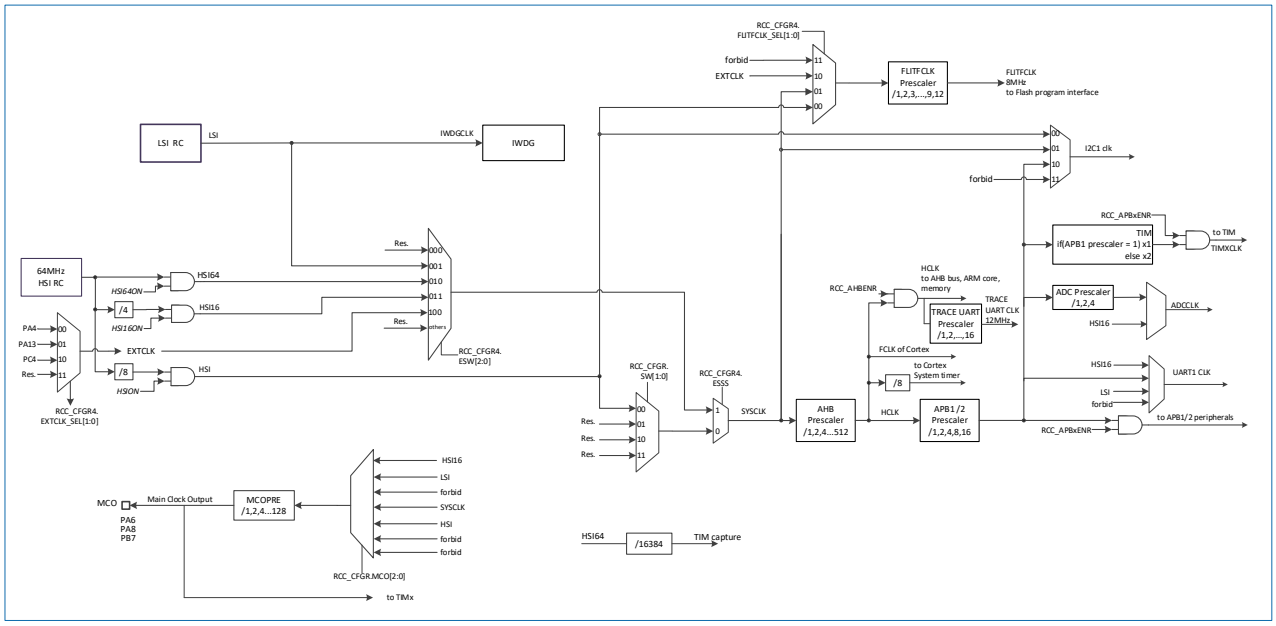

Figure 3-4 Clock tree

As the figure shows, HSI64 and ADCCLK are generated by the same internal oscillator operating at 64 MHz. Therefore, when HSI64 or ADCCLK is used, disabling the other clock cannot reduce power consumption.

HK32M050 MCUs use SYSCLK as the CPU clock when they start. The internal oscillator outputs a 64 MHz clock. The HSI divided from this 64 MHz clock is used as the default system clock when the MCU is powered on. HSI/HSE can be used as the input of the phase-locked loop (PLL) prescaler. You can use HSI/HSE together with PLL to configure different system clock frequencies.

HK32M050 provides more clock sources for the system clock and offers convenient, flexible, and diverse operating modes to customers. The following clocks can act as the system clock:

- High-speed internal clock (HSI): 8/16/64 MHz
- Low-speed internal clock (LSI): 40 kHz
- GPIO external input clock: 5 MHz to 30 MHz

The clock frequency of the AHB and the APB domain can be configured by using several prescalers. The maximum clock frequency of the AHB can be 64 MHz. The maximum clock frequency of the APB domain can be 64 MHz.

3.9 GPIO

Each GPIO pin can be configured as an output pin (push-pull or open-drain), an input pin (floating, pull-up, or pull-down), or assigned to a peripheral alternate function by using the software. Most of the GPIO pins are shared by the digital and analog alternate functions. The configuration of I/O alternate functions can be locked as needed by performing a specific operation, which helps avoid unexpected writes to the I/O registers.

3.10 SYSCFG

The HK32M050 MCU has a set of system configuration registers. SYSCFG provides the following functions:

- Enable or disable the fast mode plus of I2C on some I/O ports.
- Remap the memory areas.
- Manage external interrupts connected to GPIOs.
- Manage the remapping of LSI, HSI64/16384 signals to TIM3_CH4.
- Manage the switch controlling the output of some internal analog signals to I/Os.
- Configure the internal voltage divider (8-bit DAC).

3.11 Interrupts and events

3.11.1 NVIC

HK32M050 incorporates the nested vectored interrupt controller (NVIC). NVIC can flexibly manage up to 16 maskable interrupt channels (excluding 16 Cortex®-M0 interrupt lines) and four interrupt priorities while maintaining the lowest interrupt latency.

- The NVIC closely coupled with the core interface ensures low latency in interrupt processing.
- The interrupt entry vector address is directly passed to the core.
- Supports the early processing of interrupts.
- Processes late-arriving interrupts that have higher priorities.
- Supports tail-chaining.
- The processor state is automatically saved.
- The previous state is resumed upon interrupt exit with no extra instruction needed.

3.11.2 EXTI

The extended interrupt/event controller (EXTI) manages asynchronous interrupts and events. It outputs event requests to the CPU, outputs interrupt requests to the interrupt controller, and outputs wakeup requests to the power supply management module.

EXTI can be categorized into edge-configurable EXTI and edge-fixed EXTI. For the edge-fixed EXTI, only the rising edge is the trigger edge. The EXTI only operates in Stop mode and is used to wake up the core from Stop mode.

- Manages up to 16 interrupt/event requests
  - 16 edge-configurable EXTI lines
    - Configurable trigger edge: rising edge or falling edge
    - Dedicated flag for the interrupt status bit
    - Interrupts and events can be triggered by software.
  - 1 edge-fixed EXTI line
- Each interrupt/event line can be triggered and masked individually.

- Detects external signals whose pulse width is shorter than the APB2 clock period.

3.12 IWDG

The independent watchdog (IWDG) is based on a 12-bit downcounter and an 8-bit prescaler. The IWDG is clocked by an internal independent 40 kHz RC oscillator (LSI). The RC oscillator is independent of the main clock, so it can operate in Stop mode. The IWDG can reset the system when a problem occurs or work as a free-running timer to provide timeout management for applications. The IWDG can be started by hardware or software through the configuration of the option bytes. In debug mode, the counter can be frozen.

You can set the window register IWDG_WINR to use IWDG in window mode.

3.13 WWDG

The window watchdog (WWDG) is based on an internal 7-bit downcounter. The counter can be set to the free running mode or used as a watchdog to reset the system when the system crashes. The WWDG is clocked by the main clock and has the early warning interrupt function. In debug mode, the counter can be frozen.

3.14 Timers

The HK32M050 MCU has an advanced timer, two general-purpose timers, and a basic timer. The following table describes the functions of timers.

Table 3-1 Functions of timers

Type	Timer	Counter Resolution	Counter Type	Prescaler Factor	Break Input	Capture/ Compare Channels	Complementary Outputs
Advanced timer	TIM1	16-bit	Up, down, up/down	1 to 65536	Yes	3	3
General-purpose timer	TIM2	32-bit	Up, down, up/down	1 to 65536	No	4	No
	TIM3	16-bit	Up, down, up/down	1 to 65536	No	4	No
Basic timer	TIM6	16-bit	Up	1 to 65536	No	No	No

3.14.1 Advanced timer

HK32M050 integrates an advanced timer TIM1.

TIM1 can be deemed as a three-phase PWM generator with six channels or used as a complete general-purpose timer. The three independent channels of TIM1 can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned mode)
- One-pulse mode output
- Complementary PWM outputs with programmable inserted dead-times

If TIM1 is configured as a 16-bit timer, it has the same functions as a basic timer. If TIM1 is configured as a 16-bit PWM generator, it has full modulation capability (0–100%). Many functions of TIM1 are the same as those of general-purpose timers. Therefore, the advanced timer can work together with general-purpose timers through the Timer Link feature for synchronization or event chaining.

The advanced timer provides the update event shifting function and simple data migration function which can be adopted in motor control.

In debug mode, the counter can be frozen.

3.14.2 General-purpose timer

HK32M050 integrates two general-purpose timers.

- TIM2 and TIM3

TIM2 is based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. TIM2 and TIM3 have four independent channels respectively. The channels can be used for input capture, output compare, PWM output, and one-pulse mode output.

TIM2 and TIM3 can work with advanced timer TIM1 through the Timer Link feature for synchronization and event chaining. TIM2 and TIM3 can generate independent DMA requests. TIM2 and TIM3 can process quadrature (incremental) encoder signals and the digital outputs from one to three hall-effect sensors. In debug mode, the counter can be frozen.

3.14.3 Basic timer

HK32M050 integrates a basic timer TIM6.

TIM6 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. In debug mode, the counter can be frozen.

3.14.4 SysTick timer

SysTick timer is a dedicated timer of the operating system. It is a standard downcounter with the following features:

- 24-bit downcounter
- Auto-reload capability
- Generates a maskable interrupt when the counter reaches 0
- Programmable clock source

3.15 ADC

HK32M050 incorporates a 12-bit analog-to-digital converter (ADC) which has a total of six external channels and five internal channels. The A/D conversions of the channels can be performed in single, continuous, scan, or discontinuous mode.

- 12-bit resolution
- The maximum ADC clock frequency is 16 MHz, and the maximum ADC conversion frequency is 1.14 MSPS.
- Flexible queue configuration: four independent regular queues
- Flexible arbitration mechanism: priorities from 0 to 3 for each queue. A larger number indicates a higher priority.
- Independent register for each channel to store the conversion result
- Channels can be changed: the conversion request of a channel can be redirected to another channel. This feature can be used to test the inputs to the same channel and save the conversion results to the registers of other channels.
- The data window comparison function enables the ADC conversion results to be compared with the preset values.
- The data averaging function performs data pre-processing.
- Supports the configuration of trigger latency. The ADC conversion starts after the latency elapsed from when the trigger signal is generated.

- The events generated by advanced timer (TIM1) and general-purpose timers (TIM2/TIM3) can be internally connected to the ADC start trigger to trigger A/D conversions.

3.15.1 Internal reference voltage

The internal reference voltage V_{REFINT} provides a stable voltage output (bandgap voltage reference) for the ADC.

3.16 COMP

HK32M050 has a built-in voltage comparator (COMP). This comparator can be used independently or used with timers.

This comparator can be used:

- To wake up the MCU from low-power modes after being triggered by the analog signal.
- For analog signal conditioning.
- Together with the timer PWM output to form the cycle-by-cycle current control loop.

3.17 OPAMP

HK32M050 integrates two operational amplifiers (OPAMPs). They can operate in Standalone, Follower, and PGA modes.

The outputs of OPAMPs can be output to pins, internally connected to the inverting input node, or strobed in the internal ADC for sampling.

3.18 EMACC

Electric motor acceleration (EMACC) can be used on brushless direct current (BLDC) motors controlled by the field-oriented control (FOC) algorithm. EMACC accelerates the mathematical operations of motor drives. Mathematical operations can be completed at a speed higher than that of software-based mathematical operations while occupying fewer CPU resources. The EMACC-embedded MCUs support higher motor rotation speeds and improved drive frequencies under the same CPU frequency.

On HK32M050 MCUs, the coordinate rotation digital computer (CORDIC) algorithm, Clarke, Park, and Inverse Park transformations, proportional-integral-derivative (PID) control, and space vector pulse width modulation (SVPWM) module of the FOC algorithm are based on hardware. This helps free up CPU resources and speed up computing. Users input Ia, Ib, and the θ electrical angle. After the processing by EMACC, the output of SVPWM, such as the PWM duty cycle of A, B, and C phases, can be obtained. EMACC further decreases the time consumed by the FOC algorithm.

HK32M050 contains a data tracker (EMACC_TRACE) which is a hardware high-speed serial interface module. During the motor commissioning or high-speed running process, EMACC_TRACE outputs EMACC parameters in real time. In addition, four bytes are provided for the output of user-defined data, which facilitates motor commissioning.

EMACC can significantly increase algorithm efficiency.

3.19 DVSQ

The division and square root (DVSQ) calculation unit has the following features:

- Supports the 32-bit signed integer division (SDIV), unsigned integer division (UDIV), and root calculation.
  - Supports either the division or root calculation at one time.
  - The quotient and remainder of 32-bit SDIV and UDIV are updated to the corresponding register.
  - The MOD operation is supported in division.
- High-precision root calculation can be selected for unsigned integer root calculation by using the software.

- In the streamlined design, a 2-bit calculation is completed in each clock period.
- The calculation time varies based on the calculation data.
- Supports divide-by-zero interrupt and overflow interrupt.

3.20 I2C bus

HK32M050 has an I2C bus interface that can work in multimaster mode or slave mode. The I2C interface supports the standard mode (up to 100 kHz), fast mode (up to 400 kHz), and fast mode plus (up to 1 MHz).

The I2C interface provides hardware support for SMBus 2.0 and PMBus 1.1: ARP capability, host notify protocol, hardware CRC (PEC) generation and verification, timeout verification, and ALERT protocol management.

The I2C interface has a clock independent of the CPU clock domain, so it can wake up the MCU from Stop mode when the address is matched.

Table 3-2 I2C features

I2C Feature	I2C1
Master/Slave mode	Supported
Multimaster mode	Supported
Standard/Fast/Fast mode plus	Supported
7-bit/10-bit addressing mode	Supported
General call	Supported
Event management	Supported
Clock stretching	Supported
Software reset	Supported
Analog and digital filter	Supported
SMBus2.0	Supported
PMBus1.1	Supported
Independent clock	Supported
Wakeup from Stop mode	Supported

3.21 UART

A universal asynchronous receiver-transmitter (UART1) is embedded in each HK32M050 MCU. It can communicate at up to 8 Mbit/s. The UART provides hardware management of multiprocessor communication mode and single-wire half-duplex communication mode.

Table 3-3 UART features

UART Mode/Feature	UART1
Data word length	7/8/9-bit
Multiprocessor communication	Supported
Single-wire half-duplex communication	Supported
RS232 hardware flow control	Not supported
RS485 driver enable	Not supported

3.22 SPI

A serial peripheral interface (SPI) is embedded in each HK32M050 MCU. The SPI interface supports full-duplex and half-duplex communication in master or slave mode. The 3-bit prescaler generates eight frequencies of master mode. Each frame can be configured to 4-bit to 16-bit.

Table 3-4 SPI features

SPI Feature	SPI1
Hardware CRC calculation	Supported
RX/TX FIFO	Supported
NSS pulse mode	Supported
TI mode	Supported

3.23 96-bit UID

The 96-bit unique identifier (UID) provides a reference number for each HK32M050 MCU. The UID is unique in any circumstances. You are not allowed to modify the UID. The 96-bit UID can be read in bytes (8 bits), half words (16 bits), or words (32 bits) for different applications. The 96-bit UID can be used:

- As a serial number. For example, as a USB string serial number or used for other terminal applications.
- As a security key. When programming the Flash, use the UID together with software encryption and decryption algorithms to enhance the security of code in the Flash.
- To activate the boot process of the security mechanism.

3.24 Debug port (DBG)

Based on the ARM SWJ-DP embedded in HK32M050, SWDIO/SWCLK functions are available.

4 Electrical characteristics

4.1 Absolute maximum values

The absolute maximum values are stress test values within a short period.

Caution:

- Do not use the device in conditions equal to or exceeding the absolute maximum values.
- Stresses beyond the absolute maximum values listed in Table 4-1 to Table 4-3 may cause permanent damage to the device.
- If the device works under the maximum values for extended periods, its reliability may deteriorate.

4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
$V_{DD} – V_{SS}$	External main power supply voltage (including V_{DDA} and V_{DD})	–0.3	5.5	V
V_{IN}	Input voltage on pins	–0.3	5.5	
$\|V_{SSX} – V_{SS}\|$	Variation between different ground pins	-	50	mV

4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} (source)(1)	105	mA
I_{VSS}	Total current from V_{SS} (sink)(1)	105	
I_{IO}	Output current sunk by any I/O and control pin	60	
	Output current sourced by any I/O and control pin	60	
$I_{INJ(PIN)}$(2)	Injected current on pins(3)	–5/+0	
$\Sigma I_{INJ(PIN)}$	Total injected current (all I/Os and control pins)(4)	–25/+0	

(1). All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must be connected to the external power supply within the permitted range all the time.

(2). Negative injected current causes the analog performance of the device to fluctuate.

(3). When V_{IN} is larger than V_{DD}, a positive injected current is induced; when V_{IN} is smaller than V_{SS}, a negative injected current is induced. The injected current must be within the permitted range.

(4). If multiple I/Os have current injection simultaneously, the maximum $\sum I_{INJ(PIN)}$ is the sum of the absolute instantaneous values of positive and negative injected currents.

4.1.3 Temperature characteristics

Table 4-3 Temperature characteristics

Symbol	Description	Min	Max	Unit
T_{STG}	Storage temperature range	–55	130	°C
T_J	Maximum junction temperature	–55	130	°C

4.2 Operating conditions

4.2.1 Recommended operating conditions

Table 4-4 Recommended operating conditions

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	64	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	64	
f_{PCLK2}	Internal APB2 clock frequency	-	64	
V_{DD}	Standard operating voltage	2.5	5.5	V
V_{REFP} (1)	Analog operating voltage	2.5	5.5	V
T	Operating temperature	–40	105	°C

(1). V_{REFP} can be lower than V_{DD}. For example, V_{DD} = 4.2 V, V_{REFP} = 3.3 V; V_{DD} = 3.3 V, V_{REFP} = 2.5 V.

4.2.2 BOR characteristics

Table 4-5 BOR characteristics

Symbol	Parameter	Level	Min	Typ	Max	Unit
V_{BOR}(1)	BOR detection level selection (V_{DD} rising edge) (–40°C to 105°C)	V_{BOR1}	2.59	2.75	2.9	V
		V_{BOR2}	3	3.15	3.32	
		V_{BOR3}	3.4	3.55	3.75	
		V_{BOR4}	3.8	4	4.2	
		V_{BOR5}	4.2	4.4	4.64	
		V_{BOR6}	4.6	4.8	5.08	
	BOR detection level selection (V_{DD} falling edge) (–40°C to 105°C)	V_{BOR1}	2.44	2.6	2.88	
		V_{BOR2}	2.82	3	3.1	
		V_{BOR3}	3.19	3.4	3.5	
		V_{BOR4}	3.54	3.8	3.94	
		V_{BOR5}	3.93	4.2	4.3	
		V_{BOR6}	4.29	4.6	4.73	
$V_{BORhyst}$	BOR hysteresis	-	180	-	400	mV
t_{BORRST}(2)	Time for BOR to take effect after reaching the threshold	-	-	10	-	µs

(1). BOR is based on the monitoring of only V_{DD}.

(2). The value is guaranteed in design.

4.2.3 POR/PDR characteristics

Table 4-6 POR/PDR characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	POR/PDR threshold	Falling edge	-	2.2	-	V
		Rising edge	-	2.5	-	V
$V_{PDRhyst}$	PDR hysteresis	-	-	300	-	mV
$t_{RSTTEMPO}$(2)	Reset duration	-	-	2	-	ms

(1). PDR and POR are based on the monitoring of only V_{DD}.

(2). The value is guaranteed in design.

4.2.4 Internal reference voltage

Table 4-7 Internal reference voltage characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40°C to 105°C	-	0.8	-	V

4.2.5 Operating current characteristics

Table 4-8 Operating current characteristics

Symbol	Mode	Condition	V_{DD} = 5 V			Unit
			–40°C	25°C	105°C	
I_{run}	Run mode	SYSCLK = **64** MHz; LSI enabled, other peripherals disabled; All I/Os configured in high impedance; **Two** wait states to access Flash.	6.72	6.96	7.25	mA
		SYSCLK = **8** MHz; LSI enabled, other peripherals disabled; All I/Os configured in high impedance; **Zero** wait states to access Flash.	2.78	2.88	2.97	mA
		SYSCLK = **40** kHz; LSI enabled, other peripherals disabled; All I/Os configured in high impedance; **Zero** wait states to access Flash.	0.768	0.798	0.884	mA
I_{Sleep1}	Sleep mode 1	SYSCLK = **64** MHz; AHB/APB enabled; All clocks in the core domain disabled, all peripherals disabled; All I/Os configured in high impedance; SRAM and peripheral data retained.	4.25	4.4	4.65	mA
		Wakeup time	-	396	-	ns
I_{Sleep2}	Sleep mode 2	SYSCLK = **8** MHz; AHB/APB enabled; All clocks in the core domain disabled, all peripherals disabled; All I/Os configured in high impedance; SRAM and peripheral data retained.	1.44	1.48	1.62	mA
		Wakeup time	-	2.85	-	µs
I_{Sleep3}	Sleep mode 3	SYSCLK = **40** kHz; AHB/APB enabled; All clocks in the core domain disabled, all peripherals disabled; All I/Os configured in high impedance; SRAM and peripheral data retained.	0.353	0.404	0.509	mA
		Wakeup time	-	322	-	µs
I_{Stop}	Stop mode	All clocks stopped, HSI oscillator and HSE oscillator disabled, LSI oscillator enabled, all peripherals disabled; LDO operating in **normal power** mode; All I/Os configured in high impedance; Backup registers retained; CPU, SRAM, and peripheral data retained.	347.2	377	487	µA
		Wakeup time	-	2.9	-	µs
I_{LPstop}	Low-power stop mode	All clocks stopped, HSI oscillator and HSE oscillator disabled, LSI oscillator enabled, all peripherals disabled; LDO operating in **low-power** mode, all peripherals disabled; All I/Os configured in high impedance; Backup registers retained; CPU, SRAM, and peripheral data retained.	9.5	11.3	49.2	µA

Symbol	Mode	Condition	V_{DD} = 5 V			Unit
			–40°C	25°C	105°C	
		Wakeup time	-	100	-	µs

4.2.6 HSI clock characteristics

Table 4-9 HSI clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}(1)	Frequency	-	-	64	-	MHz
$DuCy_{(HSI)}$(1)	Duty cycle	-	45	50	55	%
$ACC_{(HSI)}$	Oscillator accuracy	RCC_CR register calibration completed by the user	–1	-	1	%
		Factory calibration: T_A = –40°C to +105°C	–1.5	-	0.71	
$T_{stb\ (HSI)}$(1)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	7	10	µs
$I_{DD\ (HSI)}$(1)	Oscillator power consumption	64 MHz, V_{DD} = 5 V	-	160	195	µA

(1). The value is guaranteed in design.

4.2.7 LSI clock characteristics

Table 4-10 LSI clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	-	40	-	kHz
$T_{su\ (LSI)}$(1)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	50	150	µs
$I_{DD\ (LSI)}$(1)	Oscillator power consumption	-	-	250	-	nA

(1). The value is guaranteed in design.

4.2.8 Flash memory characteristics

Table 4-11 Flash memory characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{PROG}	One-word programming time	240	-	-	µs
T_{ERASE}	Page erase time	200	-	-	ms
	Mass erase time	200	-	-	ms
I_{DDPROG}	One-word programming current	-	-	8	mA
$I_{DDERASE}$	Page/Mass erase current	-	-	9	mA
I_{DDREAD}	Read current@25 MHz	-		3	mA
N_{END}	Erasure endurance	100	-	-	Thousand cycles
t_{RET}	Data retention	10	-	-	Years

4.2.9 I/O pin input characteristics

Table 4-12 I/O pin input direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{DD} = 5 V	0.65 × V_{DD}	-	-	V
V_{IL}	Input low level voltage	V_{DD} = 5 V	-	-	0.2 × V_{DD}	V
V_{IHhys}	Input high level voltage	V_{DD} = 5 V	0.65 × V_{DD}	-	-	V
V_{ILhys}	Input low level voltage	V_{DD} = 3.3 V	-	-	0.2 × V_{DD}	V
V_{hys}	Schmitt trigger voltage hysteresis	V_{DD} = 5 V	-	-	0.2 × V_{DD}	mV
I_{lkg}	Input leakage current	V_{DD} = 5 V; 0 < V_{IN} < 3.3 V	-	5	-	nA
		V_{DD} = 5 V; V_{IN} = 5 V	-	5	-	nA
R_{PU}	Pull-up resistor	V_{IN} = V_{SS}	-	33	-	kΩ
R_{PD}	Pull-down resistor	V_{IN} = V_{DD}	-	33	-	kΩ

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_{IO}(1)	I/O pin capacitance	-	-	-	10	pF

(1). The value is guaranteed in design.

4.2.10 I/O pin output characteristics

Table 4-13 I/O pin output direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	Output high level voltage	2.5 V ≤ V_{DD} ≤ 5.5 V	0.8 × V_{DD}	-	-	V
V_{OL}	Output low level voltage	2.5 V ≤ V_{DD} ≤ 5.5 V	-	-	0.2 × V_{DD}	V

4.2.11 NRST pin characteristics

The NRST pin is connected to a pull-up resistor. Its peripheral application circuit can connect to an external RC circuit or no circuit.

Table 4-14 NRST pin input characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{Noise}	Low level ignored duration	-	-	80	ns

4.2.12 TIM timer characteristics

Table 4-15 TIM1 characteristics(1)

Symbol	Condition	Min	Max	Unit
F_{EXT}	Timer external clock frequency on CH1 to CH3	-	$f_{TIMxCLK}$/2	MHz

(1). The value is guaranteed in design. $f_{TIMxCLK}$ = 64 MHz.

Table 4-16 TIM2/3 characteristics(1)

Symbol	Condition	Min	Max	Unit
F_{EXT}	Timer external clock frequency on CH1 to CH4	-	$f_{TIMxCLK}$/2	MHz

(1). The value is guaranteed in design. $f_{TIMxCLK}$ = 64 MHz.

4.2.13 EMACC characteristics

Table 4-17 Motor drive carrier frequency characteristics

System Clock	ADC Clock	Min	Typ	Max	Unit
64 MHz	f_{ADC} = f_{PCLK}/2	-	12	20	kHz

Table 4-18 Comparison between the software and the FOC algorithm with EMACC

Item	Test Condition	Electrical Angle	Coordinate System Conversion	SVPWM	Total Time Consumption	Unit
Software-based motor library	System clock: 64 MHz	15.3	12.8	6.3	38.1	μs
EMACC-powered motor library	System clock: 64 MHz	15.3	2.2	3.4	25	μs

4.2.14 ADC characteristics

Table 4-19 ADC characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DD}	Analog power supply voltage when ADC is enabled	-	2.5	5	5.5	V
V_{REFP}	Positive reference voltage	-	2.5	5	5.5	V
V_{REFN}	Negative reference voltage	-	0	0	0	V
f_{ADC}	ADC clock frequency	-	0.3	16	28	MHz

Item	Description	Condition	Min	Typ	Max	Unit
f_S (1)	Sampling frequency	f_{ADC} = 16 MHz	-	1.142	-	MHz
f_{TRIG} (1)	External trigger frequency	f_{ADC} = 16 MHz	-	-	941	kHz
			-	-	17	Cycles
V_{AIN}	Conversion voltage range	-	V_{REFN}	-	V_{REFP}	V
R_{AIN} (1)	External input impedance	For details, see Table 4-20.				kΩ
R_{ADC} (1)	Sampling switch resistance	-	-	-	2	kΩ
C_{ADC}(1)	Sample and hold capacitance	-	-	5	-	pF
$Jitter_{ADC}$	Jitters triggered by ADC conversions	-	-	1	-	Cycles
t_S(1)	Sampling time	f_{ADC} = 16 MHz	1.5	-	239.5	Cycles
t_{CONV}(1)	Total conversion time (including sampling time)	f_{ADC} = 16 MHz; 12-bit resolution	14	-	252	Cycles

(1). The value is guaranteed in design.

(2). The value is measured based on the ADC clock. The register access latency is not taken into account.

The calculation formula of the maximum input impedance R_{AIN}:

$$\mathbf{R}_{AIN} < \frac{\boldsymbol{Ts}}{\boldsymbol{f_{ADC}} \times \boldsymbol{C_{ADC}} \times \ln(2^{N+2})} - \boldsymbol{R_{ADC}}$$

The value of N (resolution) is 12.

The allowable error can be lower than 1/4 least significant bit (LSB).

Table 4-20 Maximum input impedance values (f_{ADC} = 16 MHz)

Sampling Cycles Ts (Cycles)	Sampling Time tS (μs)	Maximum Input Impedance (kΩ)
1.5	0.094	0
7.5	0.469	7.7
13.5	0.844	15.4
28.5	1.781	34.7
41.5	2.594	51.5
55.5	3.469	69.5
71.5	4.469	90.1
239.5	14.969	306.5

Table 4-21 ADC accuracy

Symbol	Parameter	Test Condition	Typ	Max	Unit
ET	Total unadjusted error(1)	V_{DD} = V_{REFP} = 5 V, f_{ADC} = 16 MHz	-	16	LSB
EO	Offset error(2)		-	1	
EG	Gain error(3)		-	5	
ED	Differential linearity error(4)		-	2.5	
EL	Integral linearity error(5)		-	3.5	

(1). Total unadjusted error: The maximum deviation between the actual transfer curve and the ideal transfer curve.

(2). Offset error: The deviation between the first actual conversion and the first ideal conversion.

(3). Gain error: The deviation between the last ideal conversion and the last actual conversion.

(4). Differential linearity error: The maximum deviation between the actual step and the ideal step.

(5). Integral linearity error: The maximum deviation between any actual transition and the endpoint correlation line.

Note:

- ADC accuracy and negative current injection: Avoid injecting negative currents on any standard (non-robust) analog input pin. Otherwise, the accuracy of the conversion being performed on another analog input pin is greatly reduced. It is recommended that you add a Schottky diode (pin to ground) to the standard analog pins on which negative currents may be injected.
- With the restricted V_{DDA}, frequency, and temperature range, better ADC performance can be achieved.
- The data is based on characterization but not tested in production.

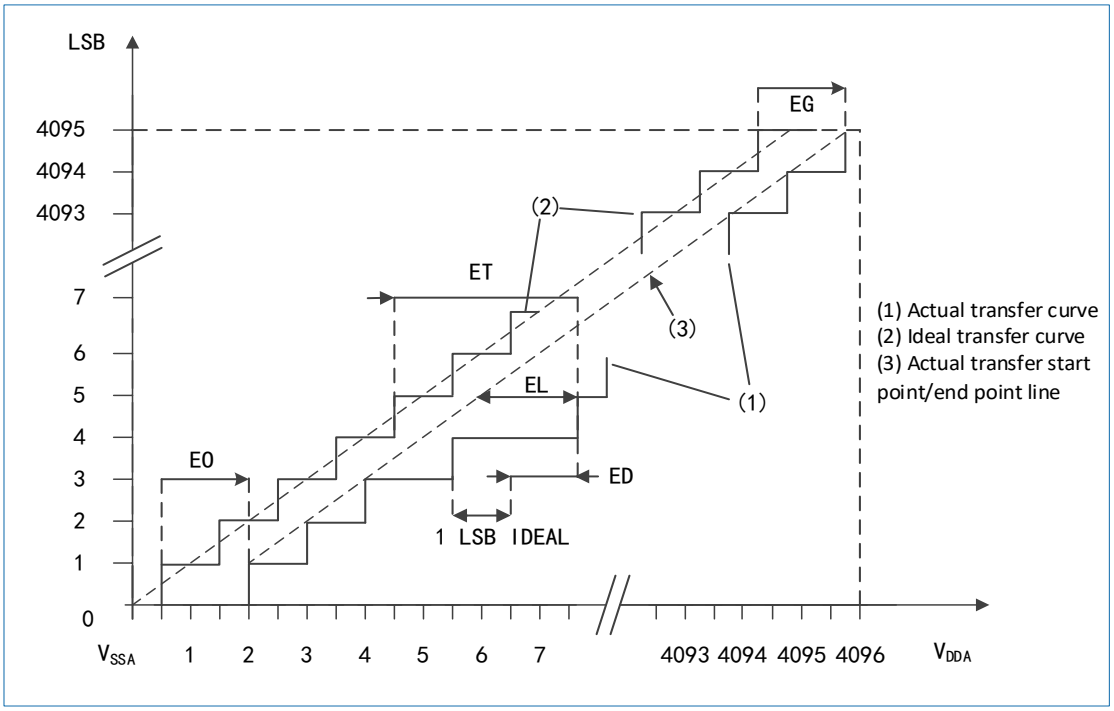

Figure 4-1 ADC accuracy characteristics

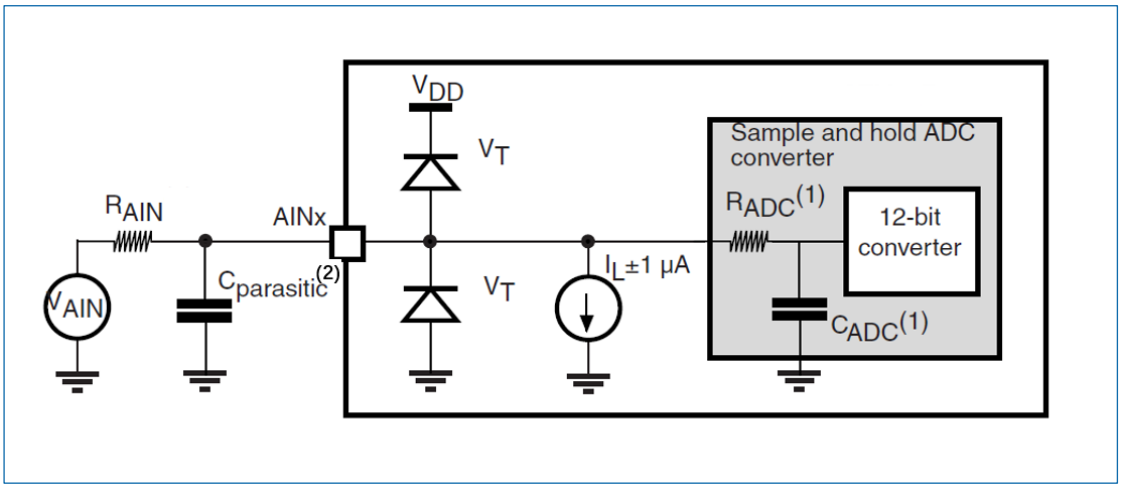

Figure 4-2 Typical connection diagram of ADC

(1). For the ADC characteristics of R_{ADC} and C_{ADC}, see Table 4-19.

(2). $C_{parasitic}$ equals the PCB capacitance (decided by soldering and the PCB layout quality) plus the pad capacitance (about 7 pF). A high $C_{parasitic}$ value reduces conversion accuracy, so f_{ADC} should be decreased.

PCB design recommendation for ADC sampling: The power supply decoupling should be performed by following Figure 5-1. To ensure the ADC conversion accuracy, the 10 nF capacitors should be ceramic and placed close to the chip.

4.2.15 DAC voltage divider characteristics

Table 4-22 DAC voltage divider characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DD}	Analog power supply voltage when DAC is enabled	-		5	5.5	V
R_O	Output impedance	-	-	-	-	kΩ
I_{OUT}(1)	Output current	-	-	-	-	mA

(1). The value is guaranteed in design.

4.2.16 Voltage comparator (COMP) characteristics

Table 4-23 COMP characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DD}	Analog power supply voltage	-	2.5	5	5.5	V
V_{com}	Input common mode voltage	-	0.2	-	5.3	V
V_{diff}	Input differential mode voltage	Low-power (low-speed) mode	-	-	40	mV
		High-power (high-speed) mode	-	-	10.5	
V_{hy}	Hysteresis voltage	Level 1	-	0	-	mV
		Level 2	-	10	-	
		Level 3	-	20	-	
I_{OP}	Operating current (V_{DD} = 5 V, static power consumption)	Low-power (low-speed) mode	1.405	2.81	3.74	µA
		High-power (high-speed) mode	22.2	38.55	42.42	
T_{dly}(1)	Output delay (no hysteresis)	High-power (high-speed) mode Rising edge	28.67	42.81	79	ns
		Low-power (low-speed) mode Rising edge	142.3	287.4	753.4	
		High-power (high-speed) mode Falling edge	30.62	57.8	72.13	
		Low-power (low-speed) mode Falling edge	206.5	597.2	849.8	

(1). The value is guaranteed in design.

4.2.17 Operational amplifier (OPAMP) characteristics

Table 4-24 OPAMP characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DD}(1)	Analog power supply voltage	-	2.7	5	5.5	V
V_{OUT}	Output voltage	-	0.2	-	V_{DDA} – 0.2	V
CMIR	Input common mode voltage	-	0.2	-	V_{DDA} – 0.2	V
I_{load}	Output current	R_L = 100 Ω, V_{DD} = 5 V	-	6	-	mA
I_q	Operating current	Static mode	-	-	807	µA
I_I(2)	Leakage current	OPAMP disabled	-	2.00	170.00	nA
V_{OS}	Input bias voltage	Before calibration	-	±15	-	mV
		After calibration	-	±2.5	-	mV
CMRR (2)	Common mode rejection ratio	-	51	-	145	dB
PSRR (2)	Power supply rejection ratio	-	41	70	109.4	dB
UGF	Unity gain bandwidth	-	6	-	-	MHz
SR	Slew rate	(5% – 95%) rising	5.213	6.251	8.061	V/µs
		(5% – 95%) falling	5.278	6.571	8.679	
ϕ	Phase margin	-	47.09	70.93	84.58	Deg
PGA gain	PGA gain	Level 1	-	1	-	Times
		Level 2	-	2	-	
		Level 3	-	5	-	
		Level 4	-	8	-	
		Level 5	-	10	-	
		Level 6	-	12	-	
		Level 7	-	16	-	
		Level 8	-	20	-	

(1). Ensure that the operating voltage of the OPAMP is from 2.7 V to 5.5 V. The operating voltage of other peripherals can be lower than 2.7 V.

(2). The value is guaranteed in design.

5 Typical circuitry

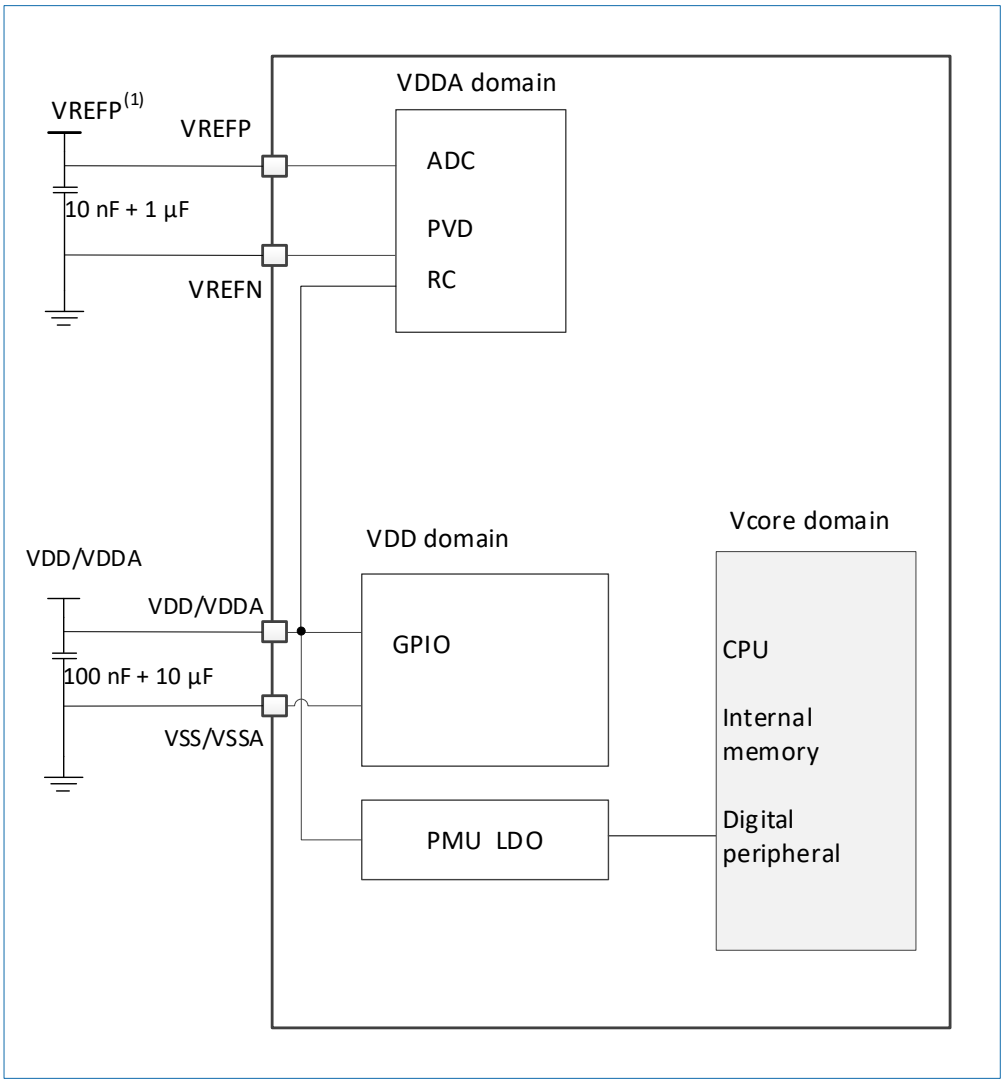

Figure 5-1 Power supply block diagram

(1). In the 28-pin package, VREFP occupies a pin exclusively. In the other packages, VREFP, VDD, and VDDA occupy a pin. For details, see section "6.7 Pin descriptions".

6 Pinouts and pin descriptions

HK32M050 MCUs are delivered in TSSOP28, QFN28, TSSOP24, QFN24, TSSOP20, and QFN20 packages. This chapter describes the pinout and pin description of each package.

6.1 TSSOP28

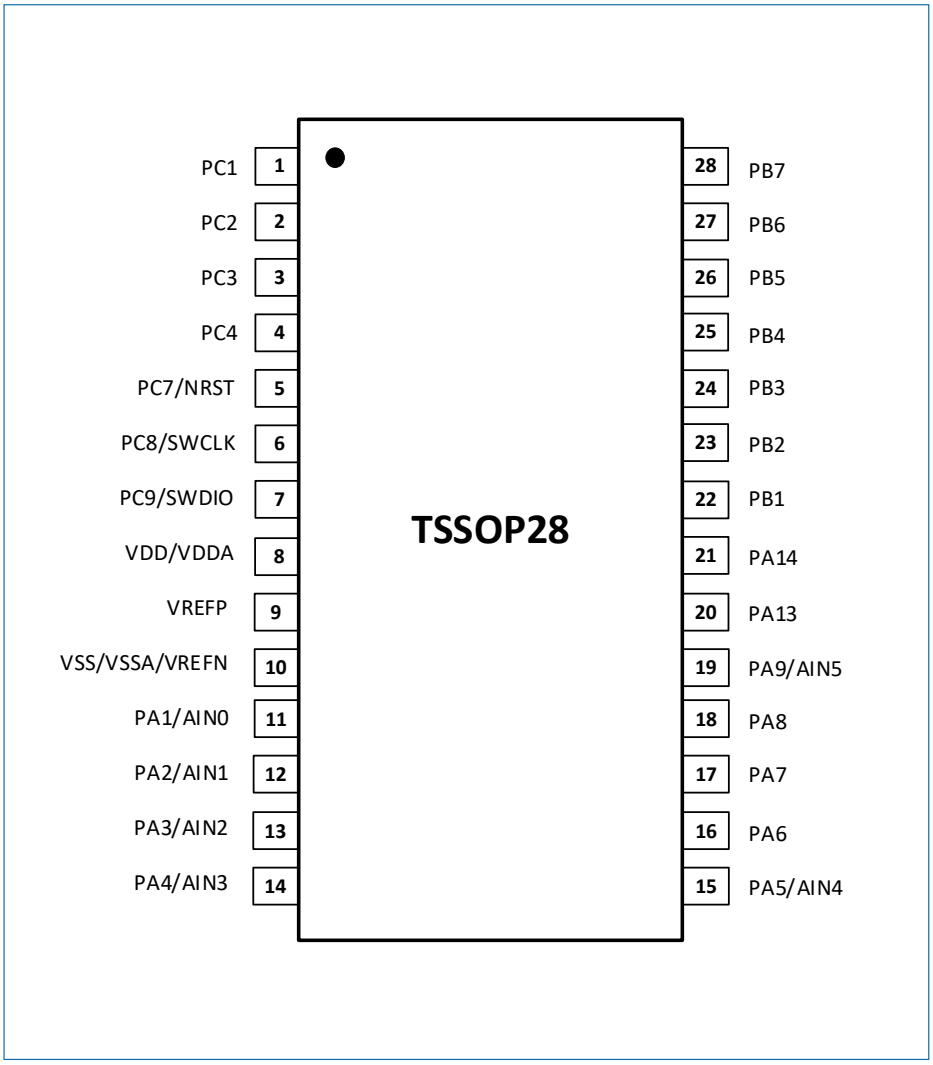

Figure 6-1 TSSOP28 package pinout

6.2 QFN28

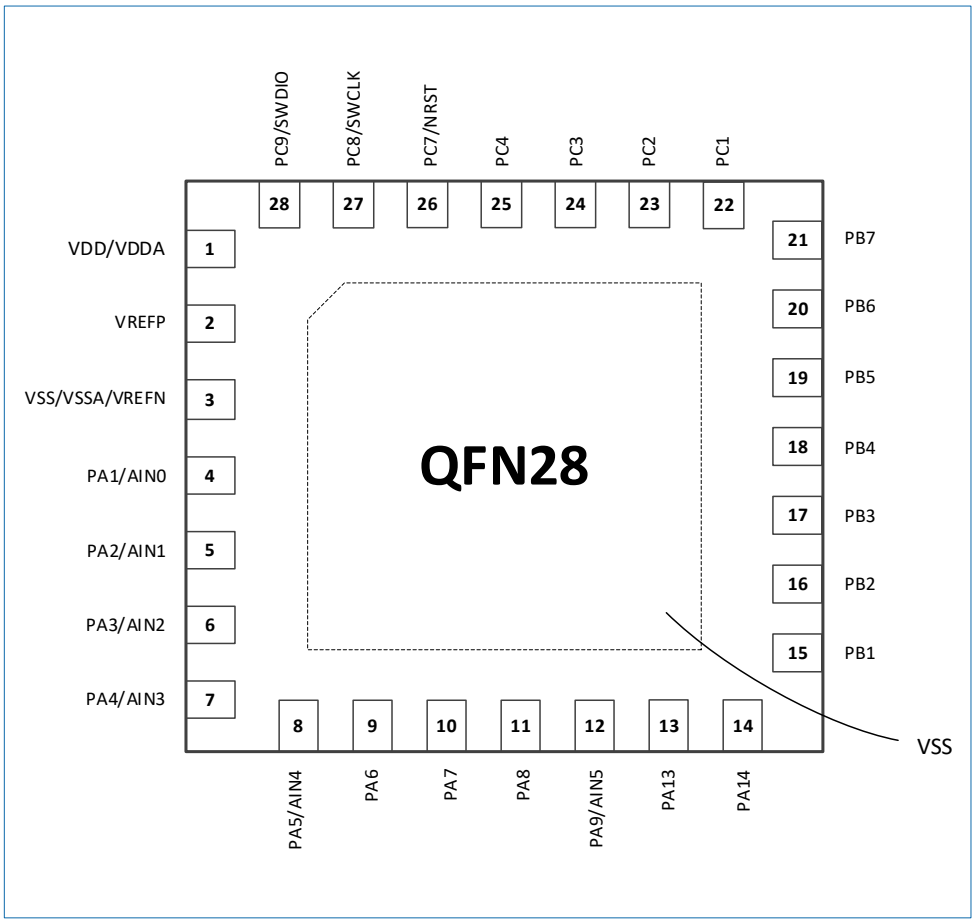

Figure 6-2 QFN28 package pinout

6.3 TSSOP24

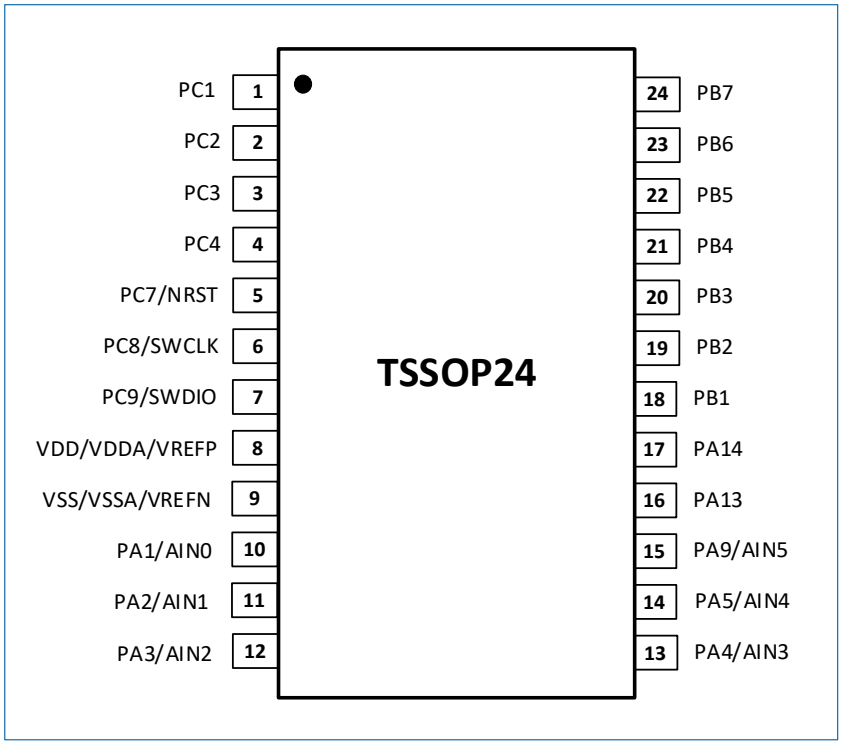

Figure 6-3 TSSOP24 package pinout

6.4 QFN24

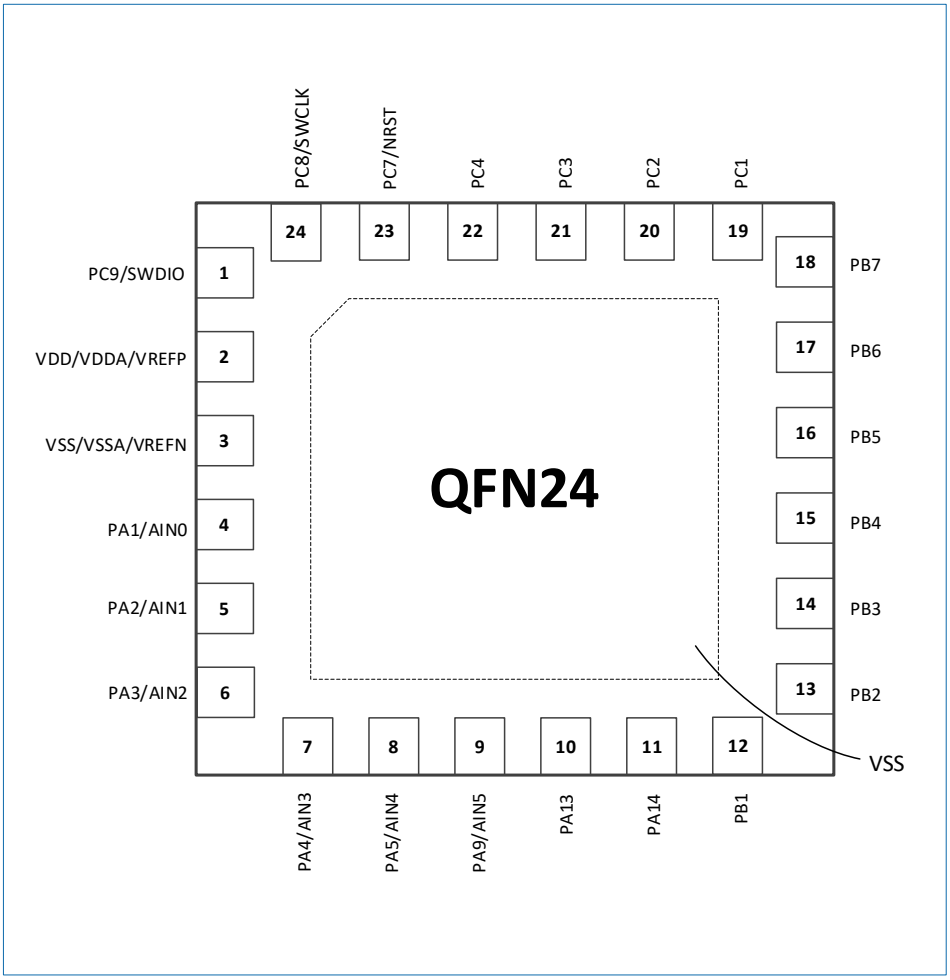

Figure 6-4 QFN24 package pinout

6.5 TSSOP20

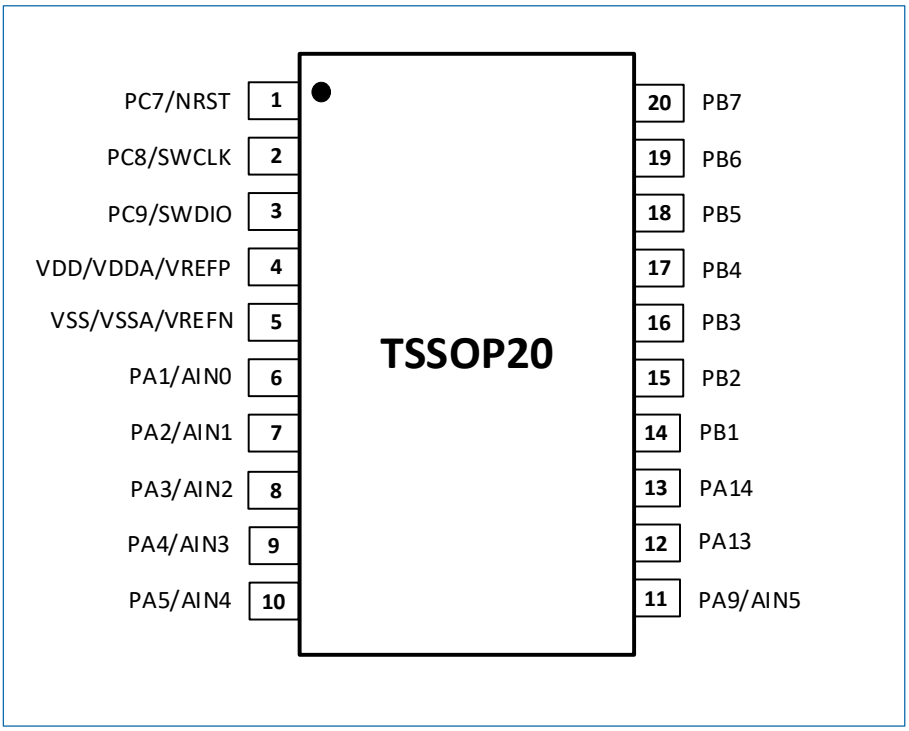

Figure 6-5 TSSOP20 package pinout

6.6 QFN20

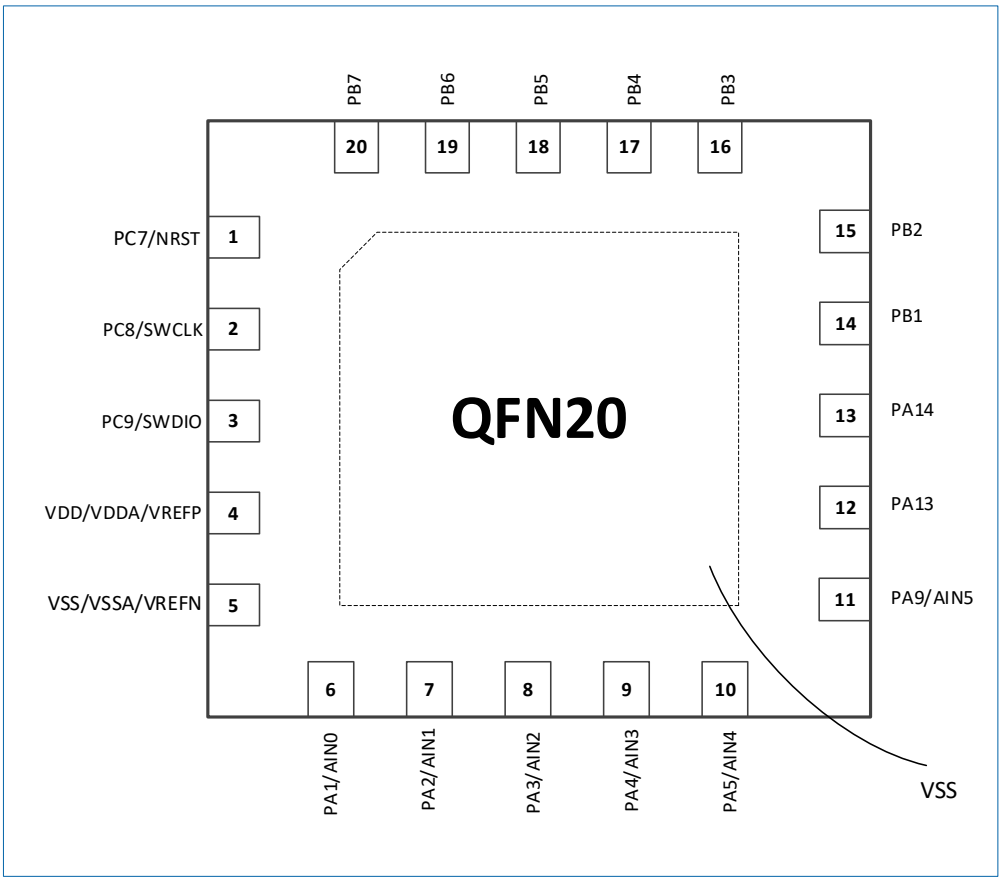

Figure 6-6 QFN20 package pinout

6.7 Pin descriptions

Table 6-1 Pin descriptions

QFN28	TSSOP28	QFN24	TSSOP24	QFN20	TSSOP20	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
0	-	0	-	0	-	VSS	S	-	Digital ground (Pin 0 is the thermal pad on the QFN package bottom.)	
1	8	-	-	-	-	VDD/VDDA	S	-	Digital/Analog power supply	
-	-	2	8	4	4	VDD/VDDA/ VREFP	S	-	Digital/Analog power supply	
2	9	-	-	-	-	VREFP	S	-	Reference power supply	
3	10	3	9	5	5	VSS/VSSA/ VREFN	S	-	Digital/Analog/Reference power supply ground	
4	11	4	10	6	6	PA1	I/O	FT (2)	TIM3_CH4 TRACE_TX	ADC_IN0 DAC1_OUT EXTIN1
5	12	5	11	7	7	PA2	I/O	FT	TIM3_CH1	ADC_IN1 OPA2_INN0 EXTIN2
6	13	6	12	8	8	PA3	I/O	FT	TIM2_CH1	ADC_IN2 OPA2_OUT EXTIN3
7	14	7	13	9	9	PA4	I/O	FT	TIM2_CH2 COMP_OUT	ADC_IN3 OPA1_INN0 EXTIN4

QFN28	TSSOP28	QFN24	TSSOP24	QFN20	TSSOP20	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
										CKI_1
8	15	8	14	10	10	PA5	I/O	FT	TIM2_CH3	ADC_IN4 OPA1_OUT EXTIN5
9	16	-	-	-	-	PA6	I/O	FT	UART1_RX I2C1_SDA MCO	COMP_INP1 OPA1_INN1 EXTIN6
10	17	-	-	-	-	PA7	I/O	FT	UART1_TX I2C1_SCL	COMP_INN0 OPA2_INN1 EXTIN7
11	18	-	-	-	-	PA8	I/O	FT	TIM3_CH1 TIM1_BKIN TIM1_ETR MCO	EXTIN8
12	19	9	15	11	11	PA9	I/O	FT	-	ADC_IN5 OPA1_INP2 OPA2_INP2 EXTIN9
13	20	10	16	12	12	PA13	I/O	FT	-	OPA1_INP1 OPA2_INP1 EXTIN13 CKI_2
14	21	11	17	13	13	PA14	I/O	FT	-	OPA_PGA_N COMP_INP0 EXTIN14
15	22	12	18	14	14	PB1	I/O	FT	-	OPA1_INP0 OPA2_INP0 EXTIN1
16	23	13	19	15	15	PB2	I/O	FT	TIM1_CH3N TIM1_CH1 TIM1_CH1N	EXTIN2
17	24	14	20	16	16	PB3	I/O	FT	TIM1_CH3 TIM1_CH2 TIM1_CH2N	EXTIN3
18	25	15	21	17	17	PB4	I/O	FT	TIM1_CH2N TIM1_CH3 TIM1_CH3N	EXTIN4
19	26	16	22	18	18	PB5	I/O	FT	TIM1_CH2 TIM1_CH1N TIM1_CH1	EXTIN5
20	27	17	23	19	19	PB6	I/O	FT	TIM1_CH1N TIM1_CH2N TIM1_CH2	EXTIN6
21	28	18	24	20	20	PB7	I/O	FT	TIM1_CH1 TIM1_CH3N TIM1_CH3 MCO	EXTIN7
22	1	19	1	-	-	PC1	I/O	FT	TIM1_CH1N TIM2_CH3 SPI_CLK MCO	EXTIN1
23	2	20	2	-	-	PC2	I/O	FT	TIM1_CH2N TIM2_CH2 SPI_CS	EXTIN2
24	3	21	3	-	-	PC3	I/O	FT	TIM1_CH3N TIM2_CH1	EXTIN3

QFN28	TSSOP28	QFN24	TSSOP24	QFN20	TSSOP20	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
									SPI_MISO	
25	4	22	4	-	-	PC4	I/O	FT	TIM3_CH1 TRACE_TX SPI_MOSI	EXTIN4
26	5	23	5	1	1	PC7/NRST (NRST)	I/O	FT	TIM1_ETR TIM1_BKIN TIM2_CH4	EXTIN7
27	6	24	6	2	2	PC8/SWCLK (SWCLK)	I/O	FT	CM0_SWCLK UART1_RX/ UART1_TX I2C1_SDA TIM3_CH2 ADC_EXT_TRIG	EXTIN8
28	7	1	7	3	3	PC9/SWDIO (SWDIO)	I/O	FT	CM0_SWDIO UART1_TX/ UART1_RX I2C1_SCL TIM3_CH3 ADC_EXT_TRIG	EXTIN9

(1). I = input, O = output, I/O = input/output, S = power supply.

(2). FT = 5 V tolerant.

Note:

- Unless otherwise specified, all I/Os are configured in analog input mode during and after resets.
- For details about alternate functions, see section "6.8 Alternate function table".

6.8 Alternate function table

Table 6-2 Alternate function table

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC8	SWCLK	ADC_EXT_TRIG	-	-	-	TIM3_CH2	UART1_RX/ UART1_TX(1)	I2C1_SDA
PC9	SWDIO	ADC_EXT_TRIG	-	-	-	TIM3_CH3	UART1_RX/ UART1_TX(1)	I2C1_SCL
PA1/AIN0	-		-	-	-	TIM3_CH4	TRACE_TX	-
PA2/AIN1	-		-	-	-	TIM3_CH1	-	-
PA3/AIN2	-		-	-	TIM2_CH1	-	-	-
PA4/AIN3	-	COMP_OUT	-	-	TIM2_CH2	-	-	-
PA5/AIN4	-	-	-	-	TIM2_CH3	-	-	-
PA6	MCO	-	-	-	-		UART1_RX(1)	I2C1_SDA
PA7		-	-	-	-		UART1_TX(1)	I2C1_SCL
PA8	MCO	-	TIM1_BKIN	TIM1_ETR	-	TIM3_CH1	-	-
PA9/AIN5	-	-	-	-	-	-	-	-
PA13	-	-	-	-	-	-	-	-
PA14	-	-	-	-	-	-	-	-
PB1	-	-	-	-	-	-	-	-
PB2	-	-	TIM1_CH3N	TIM1_CH1	TIM1_CH1N	-	-	-
PB3	-	-	TIM1_CH3	TIM1_CH2	TIM1_CH2N	-	-	-
PB4	-	-	TIM1_CH2N	TIM1_CH3	TIM1_CH3N	-	-	-
PB5	-	-	TIM1_CH2	TIM1_CH1N	TIM1_CH1	-	-	-
PB6	-	-	TIM1_CH1N	TIM1_CH2N	TIM1_CH2	-	-	-
PB7	MCO	-	TIM1_CH1	TIM1_CH3N	TIM1_CH3	-	-	-
PC1	-	-	TIM1_CH1N	-	TIM2_CH3	-	-	SPI_CLK
PC2	-	-	TIM1_CH2N	-	TIM2_CH2	-	-	SPI_CS
PC3	-	-	TIM1_CH3N	-	TIM2_CH1	-	-	SPI_MISO
PC4	-	-	-	-	-	TIM3_CH1	TRACE_TX	SPI_MOSI
PC7/NRST	-	-	TIM1_ETR	TIM1_BKIN	TIM2_CH4	-	-	-

(1). The UART RX/TX pin functions can be exchanged by configuring the UART_CR2.SWAP bit.

7 Packages

7.1 Package outlines

7.1.1 TSSOP28

TSSOP28 is a 9.70 mm × 4.40 mm, 0.65 mm pitch package.

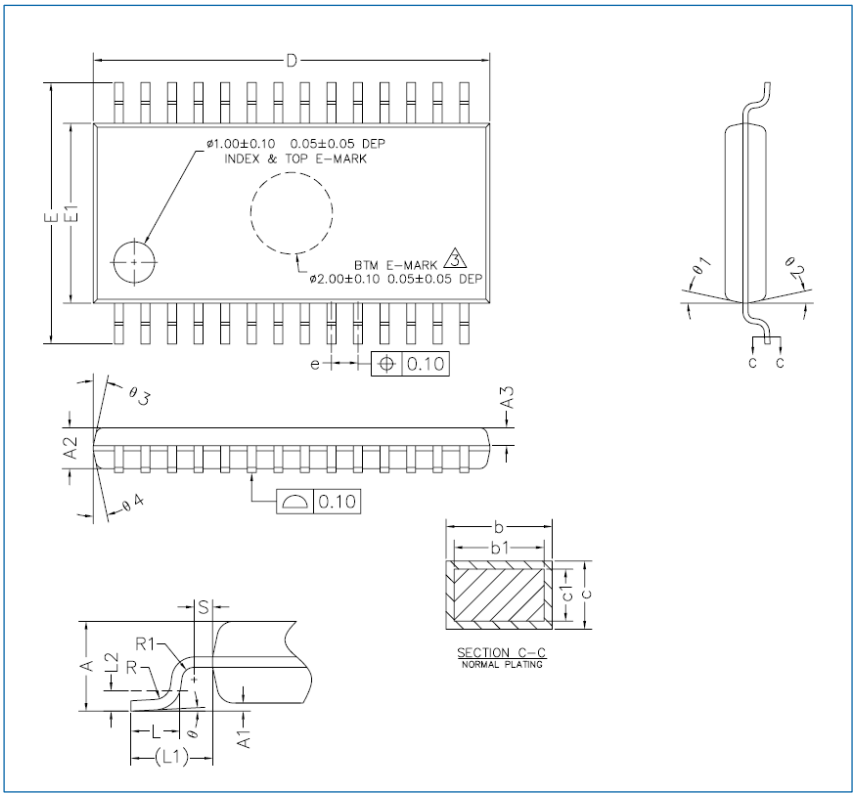

Figure 7-1 TSSOP28 package outline

Table 7-1 TSSOP28 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	-	0.29
b1	0.19	0.22	0.25
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25BSC		
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ	0°	--	8°
θ1	10°	12°	14°
θ2	10°	12°	14°
θ3	10°	12°	14°
θ4	10°	12°	14°

7.1.2 QFN28

QFN28 is a 4 mm × 4 mm, 0.4 mm pitch package.

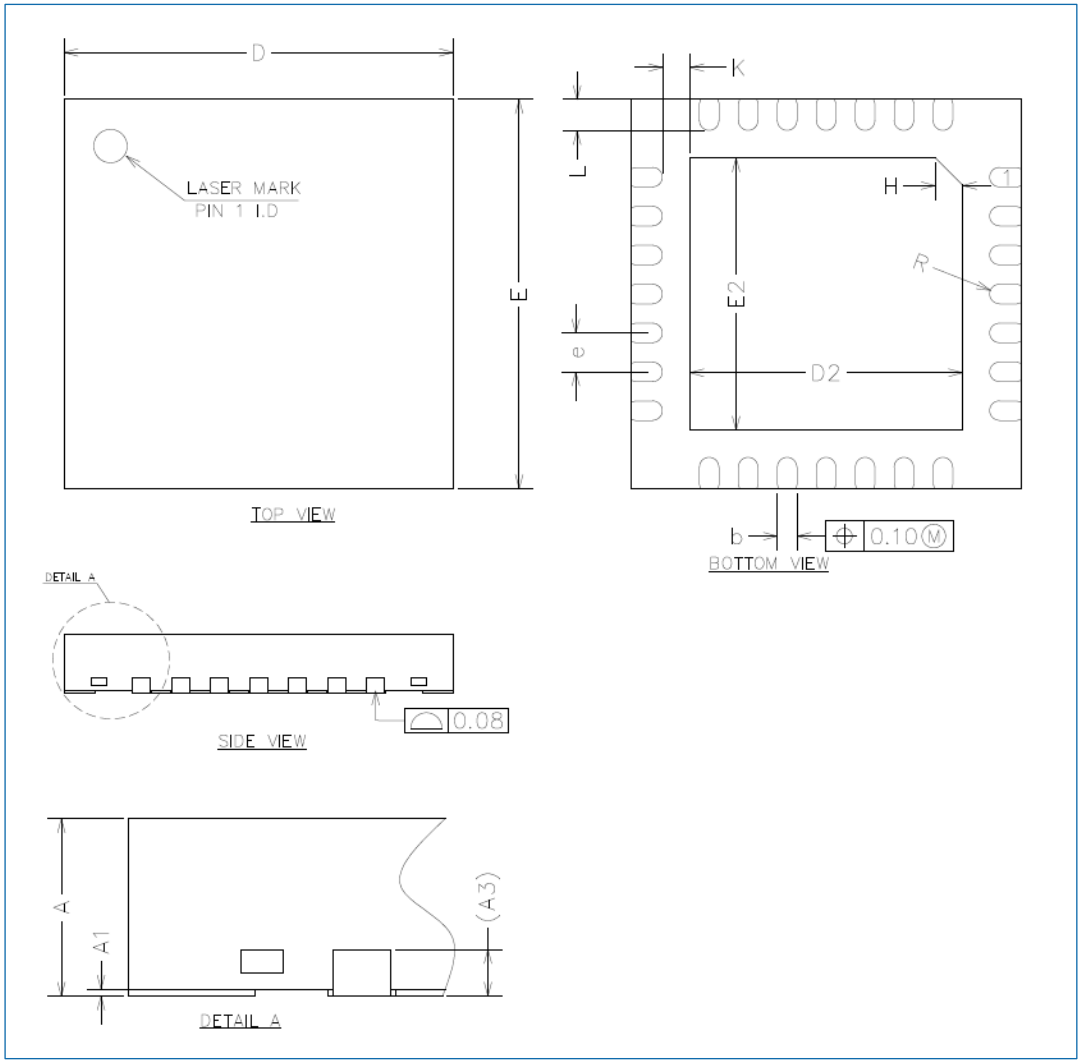

Figure 7-2 QFN28 package outline

Table 7-2 QFN28 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	0.70	0.75	0.8
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20 REF(1)		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.30	0.40	0.50
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
L	0.35	0.40	0.45
R	0.075	-	-
K	0.30 REF		
H	0.35 REF		
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.10		
eee	0.10		

7.1.3 TSSOP24

TSSOP24 is a 7.8 mm × 4.4 mm, 0.65 mm pitch package.

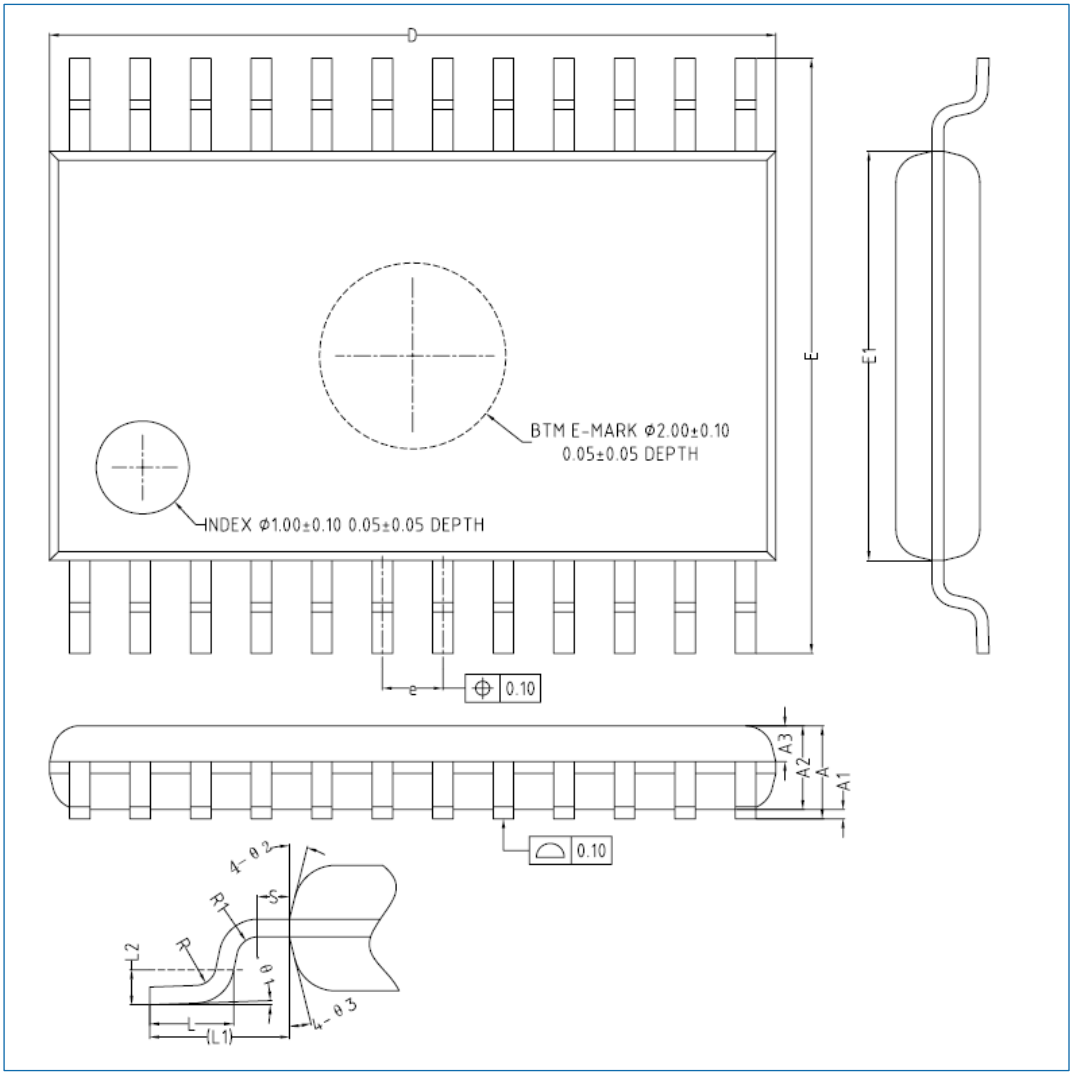

Figure 7-3 TSSOP24 package outline

Table 7-3 TSSOP24 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.00
A3	0.34	0.39	0.44
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25BSC		
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ1	0°	-	8°
θ2	12°	14°	16°
θ3	12°	14°	16°

7.1.4 QFN24

QFN24 is a 4 mm × 4 mm, 0.5 mm pitch package.

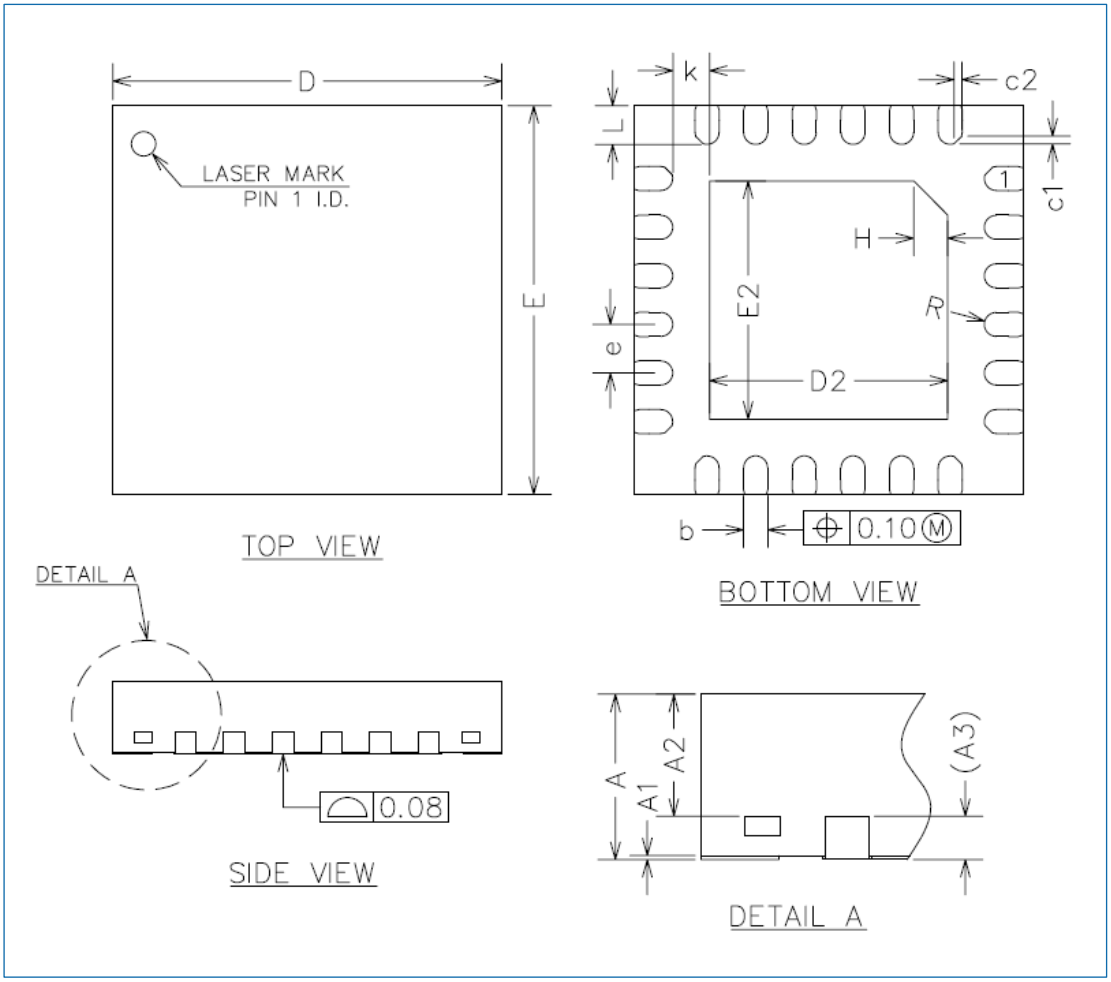

Figure 7-4 QFN24 package outline

Table 7-4 QFN24 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.127 REF		
b	0.20	0.25	0.30
D	3.95	4.00	4.05
E	3.95	4.00	4.05
D2	2.40	2.45	2.50
E2	2.40	2.45	2.50
e	0.40	0.50	0.60
H	0.35 REF		
L	0.35	0.40	0.45
K	0.20	-	-
C1	0.08 REF		
C2	0.08 REF		
R	0.09 REF		

7.1.5 TSSOP20

TSSOP20 is a 6.5 mm × 4.4 mm, 0.65 mm pitch package.

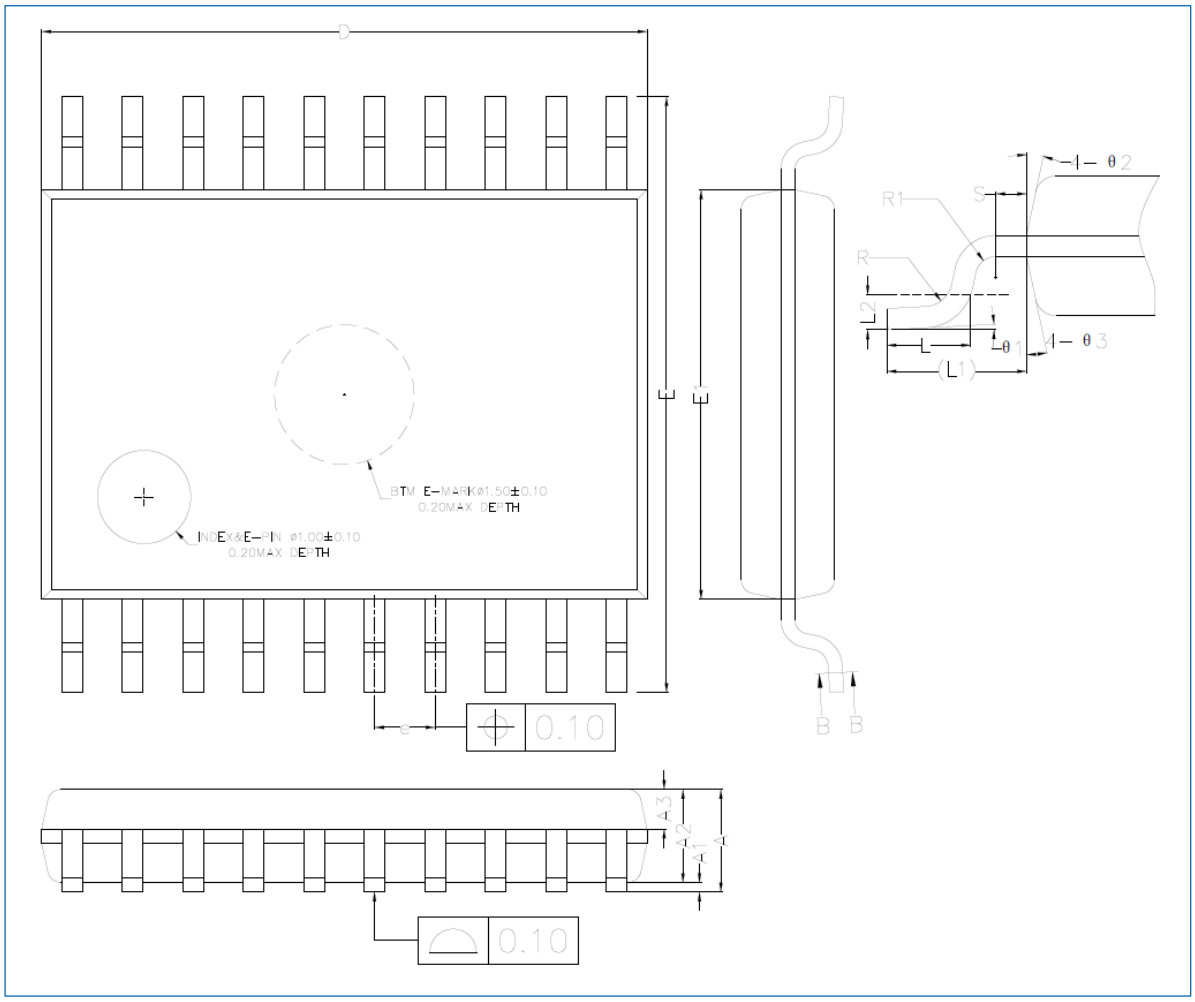

Figure 7-5 TSSOP20 package outline

Table 7-5 TSSOP20 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	-	8°

7.1.6 QFN20

QFN20 is a 4 mm × 4 mm, 0.5 mm pitch package.

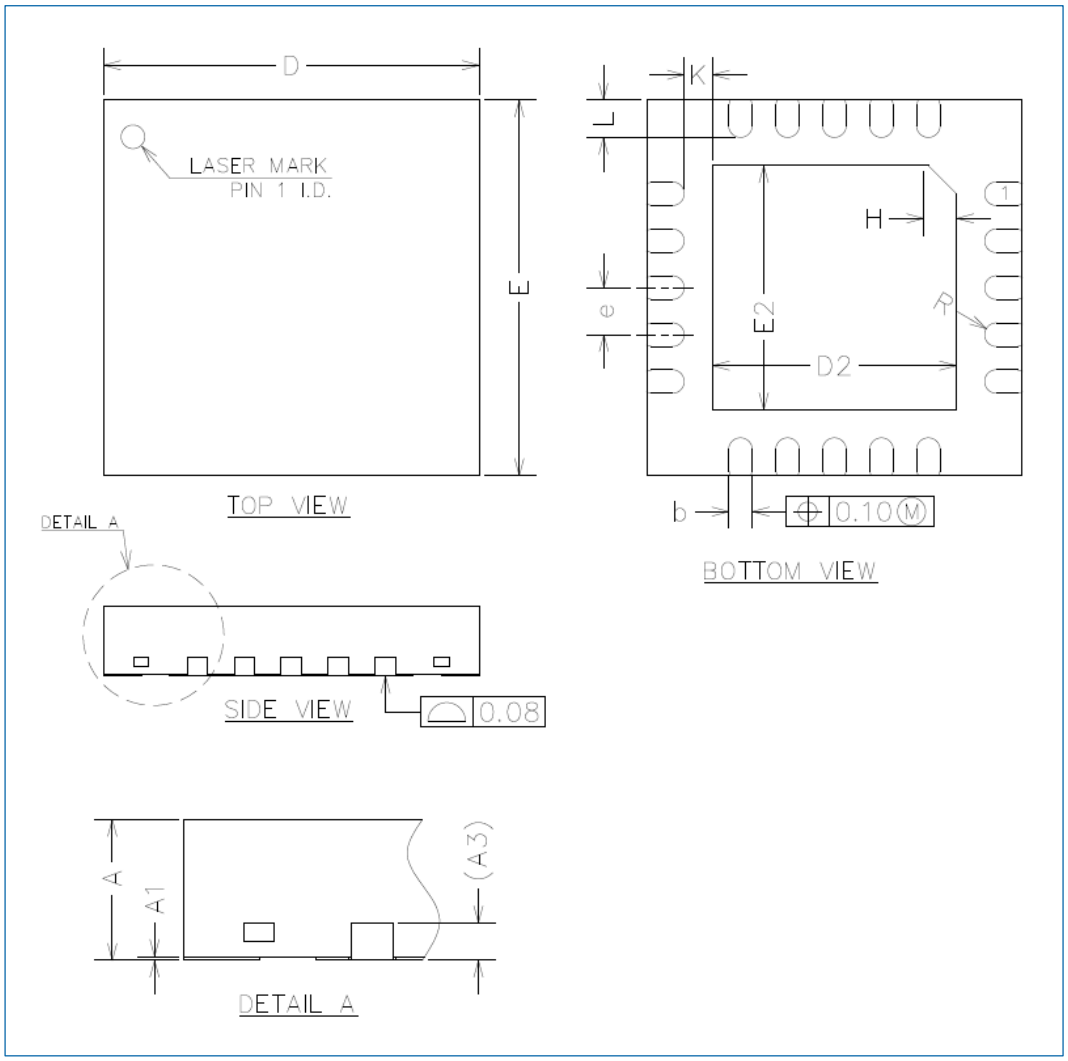

Figure 7-6 QFN20 package outline

Table 7-6 QFN20 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.2	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.15
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
e	0.40	0.50	0.60
H	0.30 REF		
K	0.20	-	-
L	0.35	0.40	0.45
R	0.10	-	-

7.2 Device marking

The device marking consists of the Hangshun logo, ARM logo, part number, and lot number. The following table describes the lot number:

Table 7-7 Lot number description

Lot Number	Description
First character	The year when the MCU was manufactured. For example, 1 indicates the year 2021.
Second and third characters	The assembly factory.
Fourth and fifth characters	The week in which the order was placed. For example, 18 indicates that the order was placed in the 18th week of the year.
Sixth, seventh, and eighth characters	The last three characters of the wafer lot number.

7.2.1 TSSOP28 marking

Figure 7-7 TSSOP28 HK32M050G4P7 marking example

7.2.2 QFN28 marking

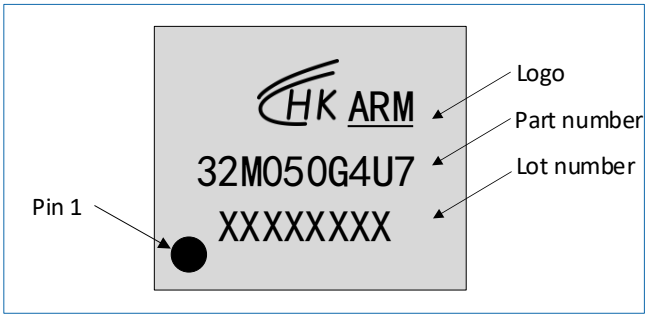

Figure 7-8 QFN28 HK32M050G4U7 marking example

7.2.3 TSSOP24 marking

Figure 7-9 TSSOP24 HK32M050E4P7 marking example

7.2.4 QFN24 marking

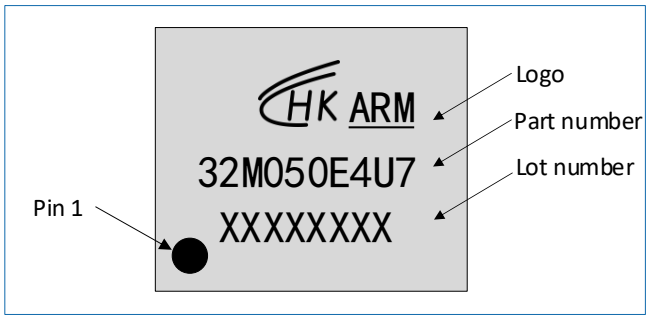

Figure 7-10 QFN24 HK32M050E4U7 marking example

7.2.5 TSSOP20 marking

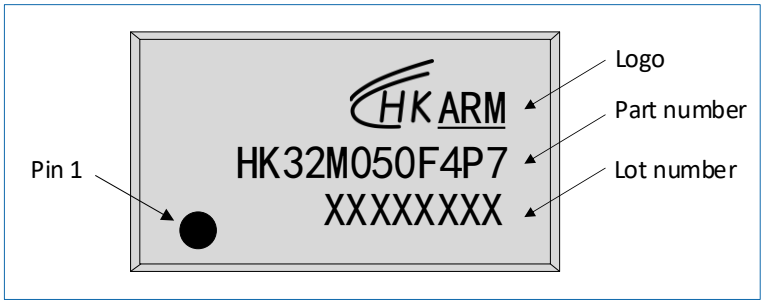

Figure 7-11 TSSOP20 HK32M050F4P7 marking example

7.2.6 QFN20 marking

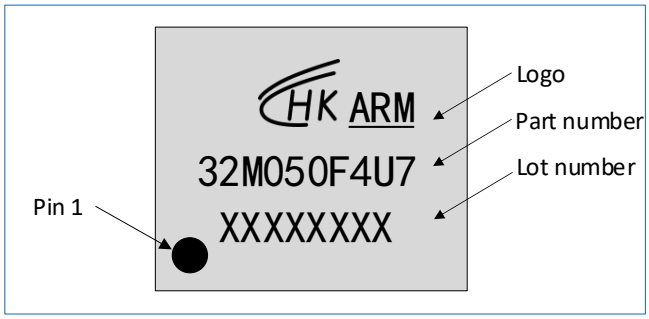

Figure 7-12 QFN20 HK32M050F4U7 marking example

8 Ordering information

8.1 Device numbering conventions

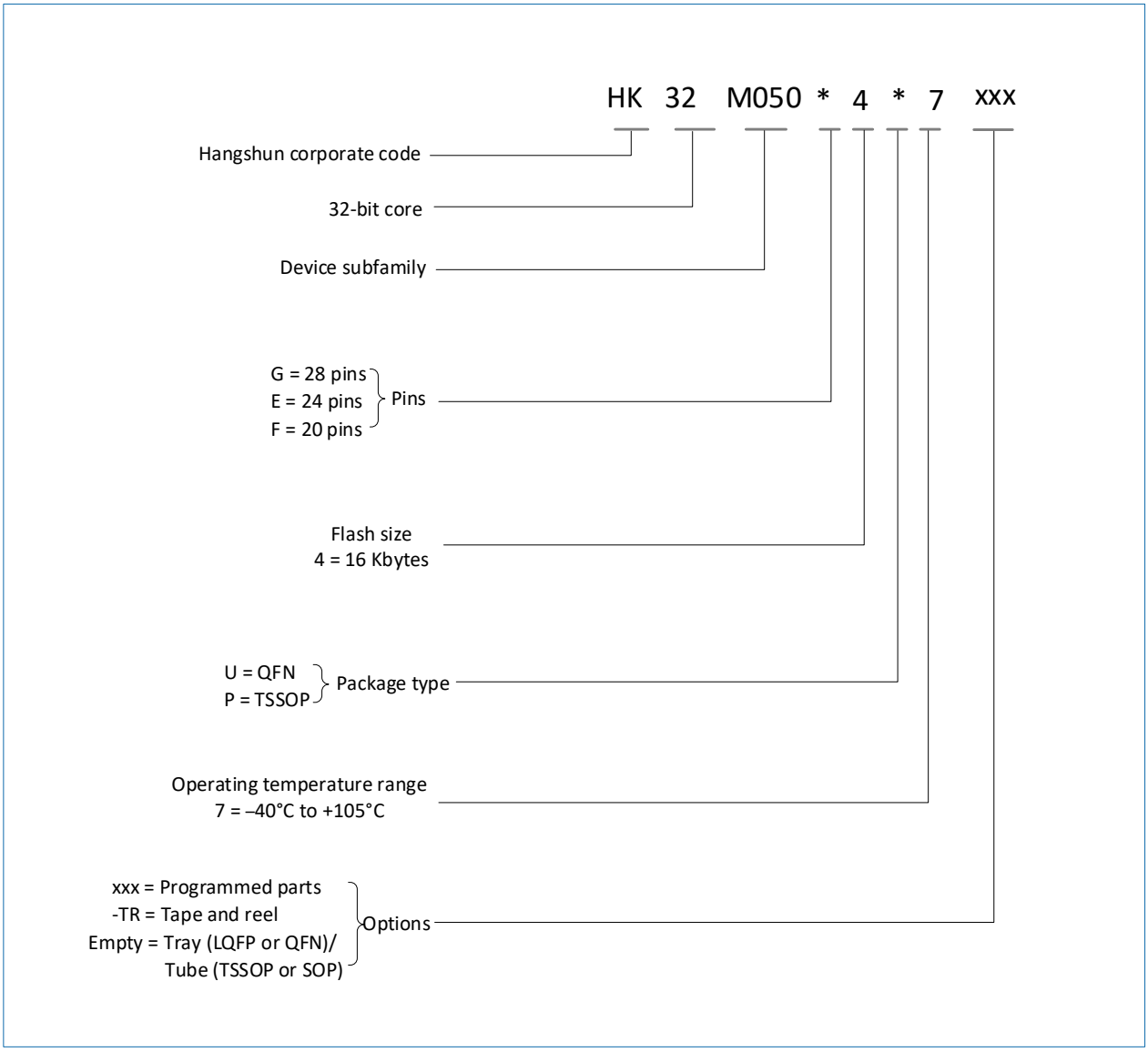

Figure 8-1 Device numbering conventions

8.2 Packaging information

Table 8-1 Packaging information

Package	Part Number	Shipping Option	Remarks
TSSOP28	HK32M050G4P7	Tube	
TSSOP28	HK32M050G4P7-TR	Tape and reel	
QFN28	HK32M050G4U7	Tray	
QFN28	HK32M050G4U7-TR	Tape and reel	
TSSOP24	HK32M050E4P7	Tube	
TSSOP24	HK32M050E4P7-TR	Tape and reel	
QFN24	HK32M050E4U7	Tray	
QFN24	HK32M050E4U7-TR	Tape and reel	
TSSOP20	HK32M050F4P7	Tube	
TSSOP20	HK32M050F4P7-TR	Tape and reel	
QFN20	HK32M050F4U7	Tray	
QFN20	HK32M050F4U7-TR	Tape and reel	

9 Acronyms

Term	Full Name
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
AWU	Auto-wakeup Unit
BLDC	Brushless Direct Current Motor
CSS	Clock Security System
CTS	Clear to Send
DMA	Direct Memory Access
EXTI	Extended Interrupt/Event Controller
FOC	Field-oriented Control
GPIO	General-purpose Input/Output
HSE	High-speed External (clock signal)
I2C	Inter-integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSI	Low-speed Internal (clock signal)
MCU	Microcontroller Unit
MSPS	Million Samples Per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-down Reset
PGA	Programmable Gain Amplifier
PLL	Phase-locked Loop
PMSM	Permanent Magnet Synchronous Motor
POR	Power-on Reset
PPM	Parts per Million
PWM	Pulse Width Modulation
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computer
RTS	Request to Send
SAR	Successive Approximation
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver/Transmitter
WWDG	Window Watchdog

10 Legal and contact information


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