HK32F030 Datasheet

Version: 1.7

Release Date: 2024-01-16

Shenzhen Hangshun Chip Technology R&D Co., Ltd.

http://www.hsxp-hk.com

Preface

Purpose

This document introduces the block diagram, memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32F030 series microcontrollers (MCUs) and helps you quickly understand the characteristics and functions of HK32F030.

Audience

This document is intended for:

- HK32F030 developers
- HK32F030 testers
- HK32F030 users

Release Notes

This document is applicable to HK32F030 series MCUs.

Revision History

Version	Date	Description
1.0.0	2018/06/08	The initial release.
1.1.0	2019/10/20	Updated section "4 Electrical characteristics".
1.2.0	2020/07/28	Update section "3.7 NVIC".
1.2.1	2020/08/21	Update section "6 Alternate function tables".
1.2.2	2021/06/21	Update section "2.2 Device overview".
1.2.3	2021/07/30	Update section "4.2.10 ADC characteristics". Added section "3.9 Resets".
1.3	2020/10/08	1. Updated the description in section "3.20 Timers": TIM14/15/16/17 all support up, down, and up/down counting modes. 2. I2C cannot wake up the MCU from Stop mode when the address is matched. Deleted the related description from the I2C section.
1.4	2022/11/03	1. Simplified the section "3.5 DVSQ calculation unit" by deleting sections "3.5.1 Division operation", "3.5.2 Square root operation", and "3.5.3 Interrupt". The operation instruction details are covered in the user manual. 2. Updated the reliability test data in section "2.1 Features". 3. Corrected grammatical errors in the whole document. 4. Changed the maximum communication rate of USART from 6 Mbit/s to 9 Mbit/s. 5. Added the description about the 96-bit UID.
1.5	2022/12/08	Corrected minor description errors.
1.6	2023/06/29	1. Updated the reliability test data. 2. Update Table 3-1 NVIC. 3. Updated the description of the Stop mode in section "3.14 Low-power modes". 4. Added the content of section "3.15 DMA". 5. Updated the package figures in section "5 Pinouts and pin descriptions" and updated section "8.2 Packaging information". 6. Added section "7.2 Device marking" and section "8.1 Device numbering conventions". 7. Updated section "4.1.1 Voltage characteristics". 8. Deleted the 7-bit configurable data format of USART. 9. Updated the number of ADC channels of HK32F030F4P6.
1.7	2024/01/16	1. Updated section "2.2 Device overview".

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Version	Date	Description
		2. Updated section "3.1 Block diagram". 3. Updated Figure 3-3 Reset signal. 4. Updated section "5.5 Pin descriptions". 5. Incorporated "GPIO alternate function tables" into chapter "5 Pinouts and pin descriptions".

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1 Introduction

This document is the datasheet for HK32F030 series MCUs. HK32F030 is a family of MCUs developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd (hereinafter referred to as Hangshun) for a wide range of purposes. This MCU family includes the HK32F030x4, HK32F030x6, and HK32F030x8 sub-series. Their part numbers include:

- HK32F030x4P6
  - HK32F030F4P6
- HK32F030x6T6
  - HK32F030C6T6
  - HK32F030K6T6
- HK32F030x8T6
  - HK32F030R8T6
  - HK32F030C8T6

For more details on HK32F030, see *HK32F030 User Manual*.

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2 Product overview

This section describes the features of HK32F030, such as the CPU core, memory, peripheral interfaces, operating current, and operating temperature.

2.1 Features

- CPU
  - ARM® Cortex™-M0
  - Maximum frequency: 72 MHz
  - 24-bit SysTick timer
  - The CPU event signal can be input to the MCU pin to realize board-level communication with the CPU of other chips.
- Operating voltage range
  - Single power domain: main power supply V_{DD} from 2.0 V to 5.5 V
- Operating temperature range: –40°C to +105°C
- Typical operating current (V_{DD})
  - Run mode: 13.23 mA@72 MHz@3.3 V
  - Sleep mode: 5.44 mA@3.3 V
  - Stop mode:
    - LDO in the low-power state: 10 µA@3.3 V
    - LDO operating at full speed: 128 µA@3.3 V
  - Standby mode: 1.64 µA@3.3 V
- Memory
  - Up to 64 Kbytes of Flash
    - No wait states to access Flash when the CPU frequency is 24 MHz or lower
    - Separate read and write protection to protect code
    - Encryption for instructions and data stored in the Flash, preventing the damage caused by physical attacks
  - 10-Kbyte SRAM (hardware verification not supported)
- Clock
  - High-speed external clock (HSE): 4 MHz to 16 MHz
  - Low-speed external clock (LSE): 32.768 kHz
  - High-speed internal clock (HSI): 8 MHz/14 MHz/56 MHz
  - Low-speed internal clock (LSI): 40 kHz
  - PLL output clock (up to 72 MHz)
  - GPIO input clock
- Reset
  - External pin reset
  - Power-on reset/Power-down reset (POR/PDR)
  - Software reset
  - Watchdog reset (IWDG and WWDG)

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- Low-power management reset
- Programmable voltage detector (PVD)
  - Adjustable eight-level thresholds for detected voltage
  - Rising edge and falling edge detection configurable
- GPIOs
  - Up to 55 GPIO pins
  - Each GPIO pin can be used as an external interrupt input
- DMA
  - 5-channel DMA controller
  - Can be triggered by multiple peripherals such as the timer, ADC, SPI, I2C, and USART
- Encryption
  - CRC calculation unit
- Data communication interfaces
  - 2 × USARTs: support synchronous transmission corresponding to SPI master mode and support modem operations. Provide the ISO7816 interface, LIN, IrDA capability, automatic baud rate detection, and the wakeup feature.
  - 2 × high-speed SPIs: support 4-bit to 16-bit programmable frames, with I2S multiplexed.
  - 2 × I2Cs: can operate in fast mode plus (1 MHz), support SMBus and PMBus.
- Timer
  - 1 × advanced timer: TIM1
  - 5 × general-purpose timers: TIM3/TIM14/TIM15/TIM16/TIM17
  - 1 × basic timer: TIM6
- RTC with the alarm function and can periodically wake up the MCU from Stop or Standby mode
- On-chip analog circuitry
  - 1 × 12-bit ADC: 16 channels for the input of external analog signals. Supports A/D conversion in continuous and scan modes at up to 1 MSPS.
  - 1 × temperature sensor: The analog output is internally connected to an independent ADC channel.
- Division and square root (DVSQ) calculation unit
  - Supports 32-bit fixed point division, with the quotient and remainder calculated
  - Supports 32-bit fixed point high-precision root calculation
- UID
  - 96-bit unique ID (UID) for each MCU
- CPU trace and debug
  - SWD debug interface
- Reliability
  - Passes HBM2000V/CDM1000V/MM200V/LU200 level tests.

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2.2 Device overview

Table 2-1 HK32F030 series features

Feature		HK32F030F4P6	HK32F030K6T6/ HK32F030C6T6	HK32F030C8T6/ HK32F030R8T6
Operating voltage		2.0 V to 5.5 V		
Operating temperature		–40°C to +105°C		
CPU	Core	Cortex®-M0		
	Frequency	72 MHz		
Memory	Flash (Kbyte)	16	32	64
	SRAM (Kbyte)	10		
DMA		5-channel (supports ADC/SPI/I2C/USART/timer)		
Clock	LSI	40 kHz		
	HSI	8 MHz/14 MHz/56 MHz		
	HSE	4 MHz – 16 MHz		
	LSE	32.768 kHz		
	PLL output clock	Supported (maximum output frequency: 72 MHz)		
	GPIO input clock	Supported		
Timer	Advanced timer	TIM1		
	General-purpose timer	TIM3/TIM14/TIM15/TIM16/TIM17		
	Basic timer	TIM6		
	SysTick timer	Supported		
	RTC	Supported		
	IWDG	Supported		
	WWDG	Supported		
Peripheral comm.	USART	1	1	2
	I2C	1	1	2
	SPI/I2S	1/1	1/1	2/2
Analog circuitry	ADC (external channels)	1 (9)	1 (10)	1 (10)/1 (16)
	Temperature sensor	1		
GPIOs		15	26/39	39/55
PVD		Supported		
DVSQ calculation unit		Supported		
Info. security	CRC	Supported		
	UID	Supported (96-bit)		
Package		TSSOP20	LQFP32/LQFP48	LQFP48/LQFP64

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3 Function description

3.1 Block diagram

ARM® Cortex®-M0 is a 32-bit RISC processor which provides an MCU platform featuring low cost, high performance, and ultra-low power consumption. It delivers outstanding computational performance and advanced system responses to interrupts. With an embedded ARM® Cortex®-M0 core, the HK32F030 family is compatible with ARM tools and software.

The following figure is the block diagram of HK32F030R8T6, which is used as an example of the HK32F030 family.

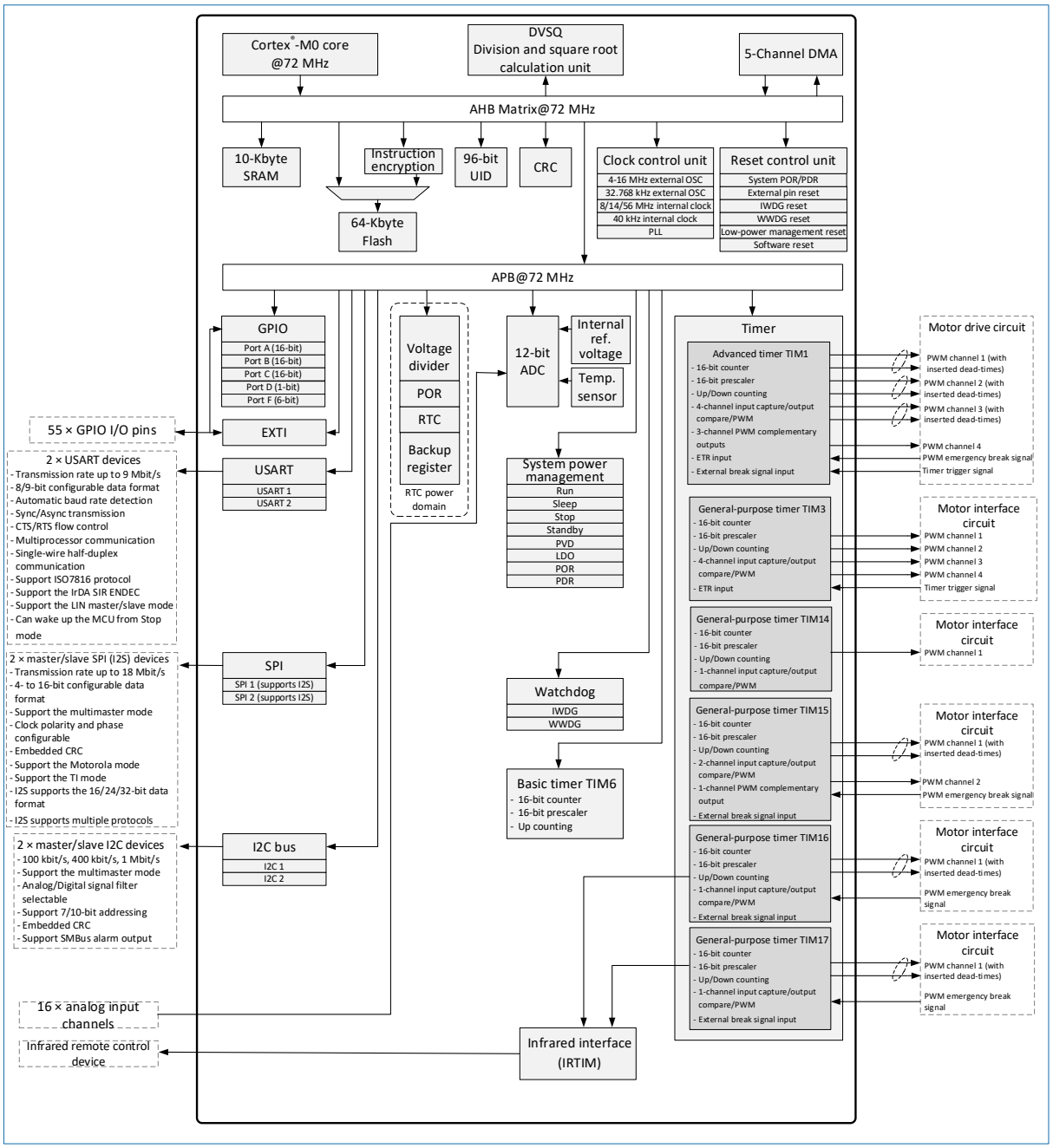

Figure 3-1 HK32F030R8T6 block diagram

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3.2 Memory mapping

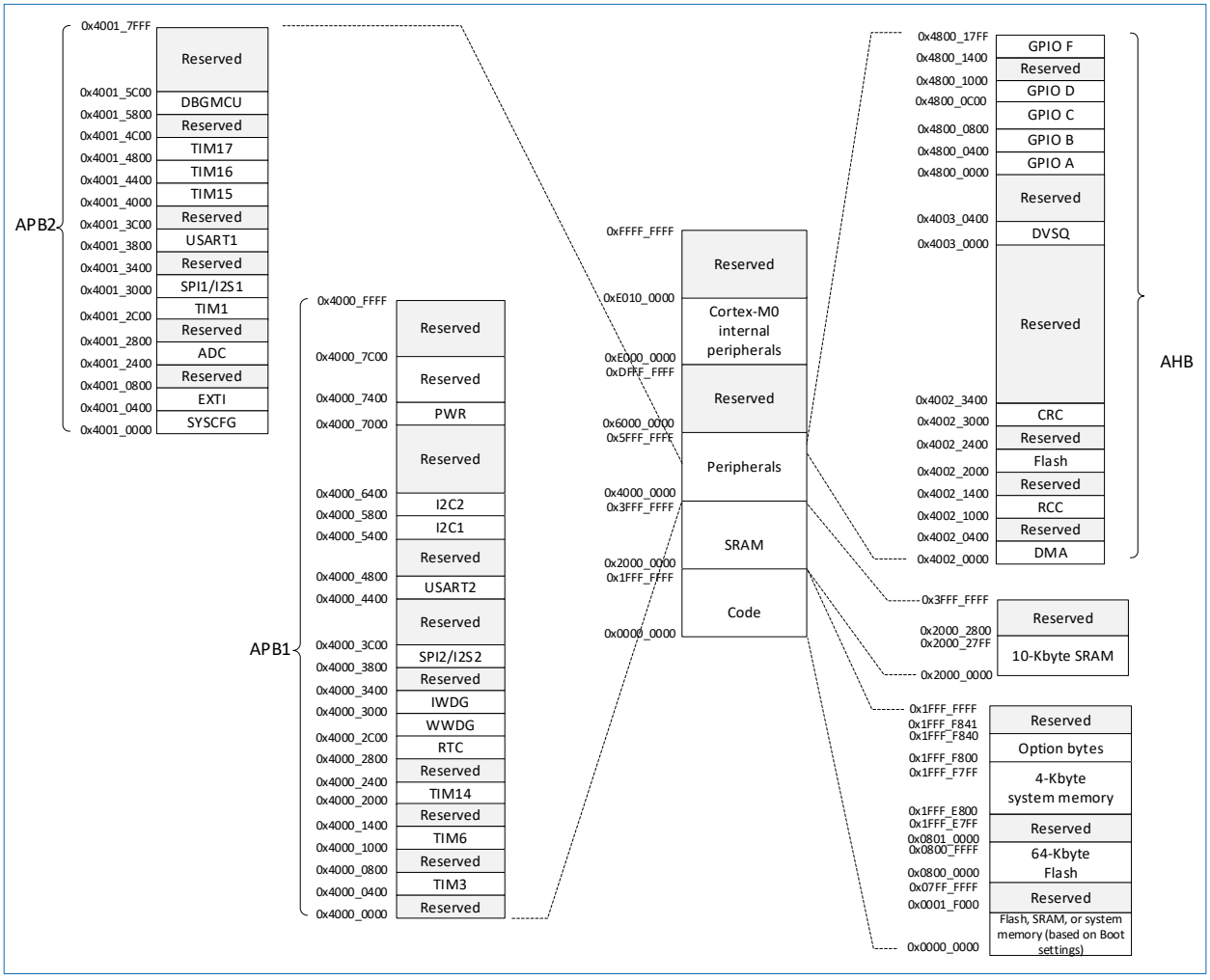

Figure 3-2 Memory mapping

3.3 Flash

HK32F030 integrates a Flash memory of up to 64 Kbytes to store programs and data.

3.4 CRC calculation unit

Cyclic redundancy check (CRC) is used to verify data integrity during transmission and storage. HK32F030 integrates a CRC calculation unit to reduce the application processing burden and accelerate processing.

The CRC calculation unit computes a signature of the software during runtime. This signature is to be compared with a reference signature, which is generated at link time and stored at a specified memory location.

3.5 DVSQ calculation unit

The division and square root (DVSQ) calculation unit has the following features:

- Supports the 32-bit signed integer division (SDIV), unsigned integer division (UDIV), and root calculation.
  - The DVSQ calculation unit supports either the division or root calculation at one time.
  - The quotient and remainder of 32-bit SDIV and UDIV are updated to the corresponding register.
  - The MOD operation is supported in division.
- High-precision root calculation can be selected for unsigned integer root calculation by using the software.
- In the streamlined design, a 2-bit calculation is completed in each clock period.
- The calculation time varies based on the calculation data.

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- Supports the divide-by-zero interrupt and overflow interrupt.

3.6 SRAM

HK32F030 has a 10-Kbyte SRAM that can be quickly accessed with no wait states, meeting the requirements of most applications.

3.7 NVIC

HK32F030 incorporates the nested vectored interrupt controller (NVIC). NVIC can flexibly manage up to 27 maskable interrupt channels (excluding 16 Cortex®-M0 interrupt lines) and four interrupt priorities while maintaining the lowest interrupt latency.

- The NVIC closely coupled with the core interface ensures low latencies in interrupt processing.
- The interrupt entry vector address is directly passed to the core.
- Supports the early processing of interrupts.
- Processes higher-priority interrupts even if they arrive late.
- Supports tail-chaining.
- The processor state is automatically saved.
- The previous state is resumed upon interrupt exit with no extra instruction needed.

Table 3-1 NVIC

Position	Priority		Name	Description	Address
-	-	-	-	Reserved	0X0000_0000
-	–3	Fixed	Reset	Reset	0X0000_0004
-	–2	Fixed	NMI	Non-maskable interrupt.	0X0000_0008
-	–1	Fixed	HardFault	All classes of faults	0X0000_000C
-	3	Configurable	SVCall	System service call via SWI instruction	0X0000_002C
-	5	Configurable	PendSV	Pendable request for system service	0X0000_0038
-	6	Configurable	SysTick	SysTick timer	0X0000_003C
0	7	Configurable	WWDG	Window watchdog interrupt	0X0000_0040
1	8	Configurable	PVD	PVD interrupt (combined with EXTI line 16)	0X0000_0044
2	9	Configurable	RTC	RTC global interrupt (combined with EXTI line 17, 19, and 20)	0X0000_0048
3	10	Configurable	FLASH	Flash global interrupt	0X0000_004C
4	11	Configurable	RCC	RCC global interrupt	0X0000_0050
5	12	Configurable	EXTI0_1	EXTI Line[1:0] interrupts	0X0000_0054
6	13	Configurable	EXTI2_3	EXTI Line[3:2] interrupts	0X0000_0058
7	14	Configurable	EXTI4_15	EXTI Line[15:4] interrupts	0X0000_005C
8	15	-	-	Reserved	0X0000_0060
9	16	Configurable	DMA_CH1	DMA1 channel 1 global interrupt	0X0000_0064
10	17	Configurable	DMA_CH2_3	DMA1 channel 2 and channel 3 global interrupt	0X0000_0068
11	18	Configurable	DMA_CH4_5	DMA1 channel 4 and channel 5 global interrupt	0X0000_006C
12	19	Configurable	ADC	ADC interrupt	0X0000_0070
13	20	Configurable	TIM1_BRK_UP_TRG_COM	TIM1 break, update, trigger, and COM interrupt	0X0000_0074
14	21	Configurable	TIM1_CC	TIM1 capture/compare interrupt	0X0000_0078
15	22	-	-	Reserved	0X0000_007C
16	23	Configurable	TIM3	TIM3 global interrupt	0X0000_0080
17	24	Configurable	TIM6	TIM6 global interrupt	0X0000_0084
18	25	-	-	Reserved	0X0000_0088
19	26	Configurable	TIM14	TIM14 global interrupt	0X0000_008C

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Position	Priority		Name	Description	Address
20	27	Configurable	TIM15	TIM15 global interrupt	0X0000_0090
21	28	Configurable	TIM16	TIM16 global interrupt	0X0000_0094
22	29	Configurable	TIM17	TIM17 global interrupt	0X0000_0098
23	30	Configurable	I2C1	I2C1 global interrupt (combined with EXTI line 23)	0X0000_009C
24	31	Configurable	I2C2	I2C2 global interrupt (combined with EXTI line 24)	0X0000_00A0
25	32	Configurable	SPI1	SPI1 global interrupt	0X0000_00A4
26	33	Configurable	SPI2	SPI2 global interrupt	0X0000_00A8
27	34	Configurable	USART1	USART1 global interrupt (combined with EXTI line 25)	0X0000_00AC
28	35	Configurable	USART2	USART2 global interrupt (combined with EXTI line 26)	0X0000_00B0
29	36	-	-	Reserved	0X0000_00B4
30	37	-	-	Reserved	0X0000_00B8
31	38	Configurable	DVSQ	DVSQ global interrupt	0X0000_00BC

3.8 EXTI

The extended interrupt/event controller (EXTI) consists of 24 edge detectors that are used to generate interrupt/event requests and wake up the system. The trigger event of each EXTI line can be independently configured to a rising edge, a falling edge, or both. Each EXTI line can be masked independently. The pending register stores the status of each interrupt request.

EXTI can detect external interrupt lines whose pulse width is shorter than the internal clock period. Up to 16 external interrupt lines are supported.

HK32F030 has 24 EXTI lines. The EXTI lines from EXTI 0 to EXTI 15 are connected to I/O pins. The connections of the other EXTI lines are as follows:

- EXTI 16 connected to the PVD output
- EXTI 17 connected to the RTC alarm event
- EXTI 19 connected to the RTC tamper detection and timestamp event
- EXTI 20 connected to the RTC wakeup event
- EXTI 23 connected to the I2C1 wakeup event
- EXTI 24 connected to the I2C2 wakeup event
- EXTI 25 connected to the USART1 wakeup event
- EXTI 26 connected to the USART2 wakeup event

EXTI lines from 23 to 26 are connected to internal events and do not have the rising trigger selection register (RTSR), falling trigger selection register (FTSR), software interrupt event register (SWIER), and pending register (PR). EXTI lines from EXTI 23 to EXTI 26 can only detect the rising edge of events in Stop mode and generate the event request (ERQ) and interrupt request (IRQ) to wake up the system.

3.9 Resets

HK32F030 supports the system reset, power reset, and backup domain reset.

3.9.1 System reset

The system reset resets all registers, except for the reset flags in the control/status register RCC_CSR and the registers in the backup domain.

A system reset is generated when any of the following events occurs:

- Low level on the NRST pin (external reset)
- Window watchdog counting terminates (WWDG reset)
- Independent watchdog counting terminates (IWDG reset)

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- Software reset (SW Reset)
- Low-power management reset

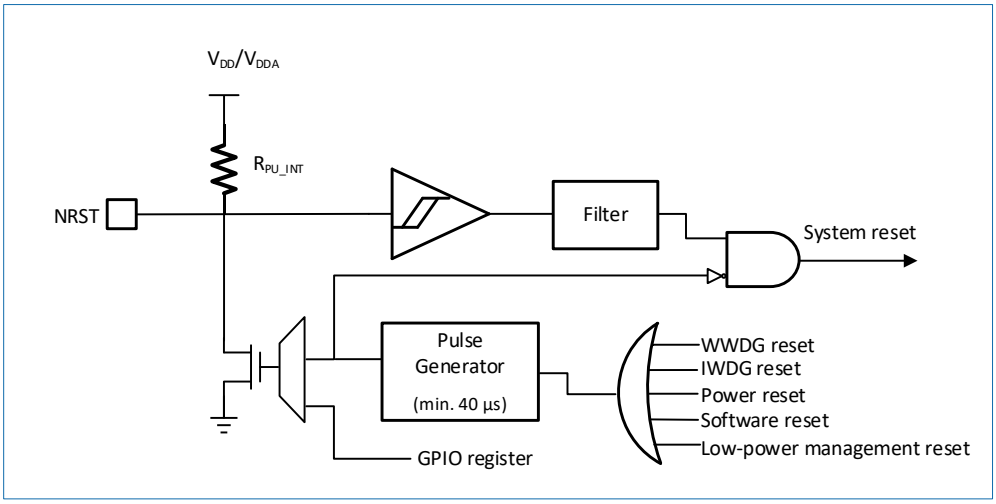

Figure 3-3 Reset signal

The internal reset signal is output on the NRST pin. The pulse generator guarantees a pulse duration of at least 40 µs for each internal or external reset source. When the NRST pin is pulled low and an external reset is generated, a reset pulse is generated.

You can identify a reset source by checking reset status flags in the RCC_CSR register.

Table 3-2 Reset setting

Reset Type	Configuration
Software reset	The SYSRESETREQ bit in Cortex®-M0 Application Interrupt and Reset Control Register must be set to 1 to force a software reset on the device.
Low-power management reset	Set the nRST_STDBY bit or nRST_STOP bit in option bytes to 0 to enable the low-power management reset. Then, even if the system is in the process of entering the Stop or Standby mode, it will be reset instead of entering the Stop or Standby mode.

3.9.2 Power reset

The power reset resets all registers, except for the registers in the backup domain. The reset sources eventually act on the reset pin. The reset pin keeps the low level during resets. The reset entry vector is fixed on address 0x0000_0004.

A power reset is generated when any of the following events occurs:

- Power-on reset (POR)/Power-down reset (PDR)
- Exit from Standby mode

HK32F030 MCUs contain the POR/PDR circuitry. The circuitry keeps operating to ensure that the system runs properly when the power supply exceeds the POR/PDR threshold. When V_{DD} is less than the POR/PDR threshold, the device is in the reset state and no external reset circuit is required.

3.9.3 Backup domain reset

The backup domain has two exclusive resets which only affect the backup domain. A backup domain reset is generated when any of the following events occurs:

- The BDRST bit in the RCC_BDCR register is set. (This also triggers the software reset.)
- V_{DD} is powered on again after being powered down (no V_{BAT}).

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3.10 Clocks

HSI and HSI14 are generated by the same 56 MHz internal oscillator. Therefore, when HSI or HSI14 is used, disabling the other clock cannot reduce power consumption. HSI can be used as the input of the phase-locked loop (PLL) prescaler. You can use HSI together with PLL to configure different clock frequencies.

All clock sources of the MCU can be selected as the system clock, including LSI and LSE. You can flexibly select the system clock based on the application power consumption and performance requirements.

The following clocks can act as the system clock:

- 32.768 kHz LSE
- 40 kHz LSI
- 56 MHz HSI
- 14 MHz HSI14
- 8 MHz HSI
- 4 – 16 MHz HSE
- PLL output clock (up to 72 MHz)
- GPIO input clock

Note:

HK32F030 provides the PCLK as one of the I2C clock sources.

The following figure shows the clock tree of HK32F030:

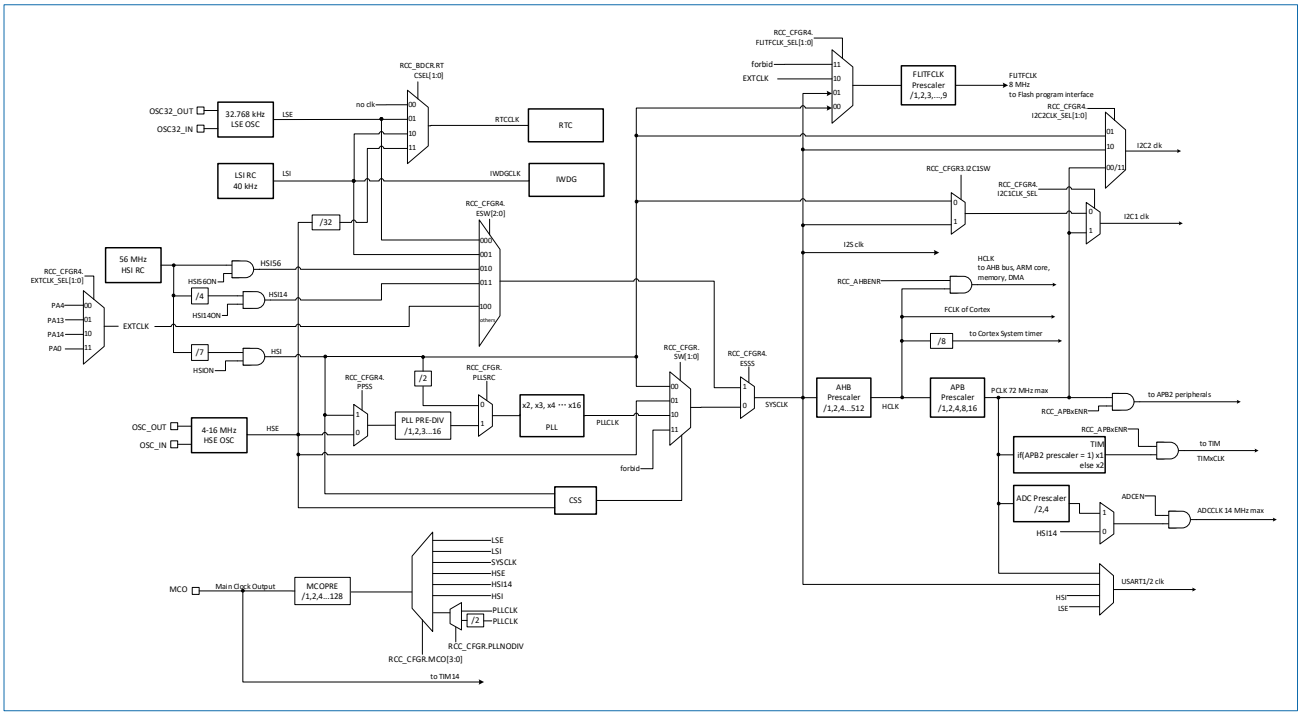

Figure 3-4 Clock tree

3.11 Boot modes

When the system starts, the boot pin is used to select one of the following boot modes:

- Boot from Flash memory
- Boot from system memory
- Boot from internal SRAM

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The bootloader program is stored in the system memory. The bootloader program can reprogram Flash via the USART interface.

3.12 Power supply scheme

- V_{DD}: 2.0 V to 5.5 V. V_{DD} supplies power to I/O pins and internal low dropout regulators (LDOs).
- V_{DDA}: 2.0 V to 5.5 V. V_{DDA} supplies power to the analog circuitry, including the ADC and temperature sensor.

Note:

HK32F030 does not have V_{BAT}. As long as there is a V_{DD} power supply, the RTC domain can operate and the Standby low-power mode is available. The following figure shows the power supply scheme:

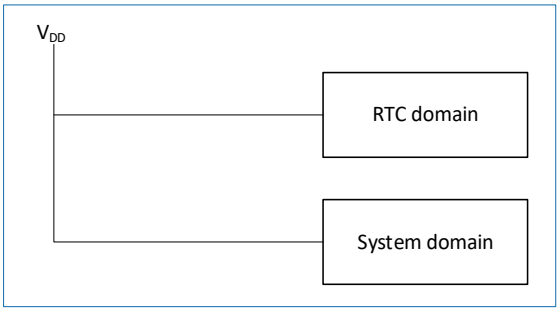

Figure 3-5 Power supply scheme

3.13 PVD

HK32F030 integrates a programmable voltage detector (PVD). The PVD monitors the V_{DD} power supply and compares it with the V_{PVD} threshold. When V_{DD} is below or over the V_{PVD} threshold, an interrupt is generated, and the interrupt program may send a warning message or set the MCU to the safe state. The PVD is enabled by setting the register.

3.14 Low-power modes

- Sleep mode

  In Sleep mode, only the CPU stops. All peripherals keep operating. The CPU can be woken up when an interrupt or event occurs.

- Stop mode

  In Stop mode, MCUs achieve the lowest power consumption while retaining the content in SRAM and registers. In Stop mode, all clocks in the core domain, the PLL, the HSE oscillator, and the HSI oscillator are disabled. MCUs can be woken up from Stop mode by an EXTI line. The EXTI line source can be any of the 16 external I/O pins, a PVD output, a USART frame header matching event, an I2C address matching event, or an RTC alarm.

- Standby mode

  In Standby mode, MCUs achieve the lowest power consumption. The internal LDO is disabled. The PLL, HSE oscillator, and HSI oscillator are also disabled. In Standby mode, the SRAM and register content is lost while the backup register content is retained. The Standby circuitry works as normal. MCUs exit from Standby mode when an external reset on the NRST pin, an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note:

For more information about the power consumption of different modes, see Table 4-6.

3.15 DMA

The general-purpose DMA controller (with five channels) manages the data transfer from memories to memories, from peripherals to memories, and from memories to peripherals. The DMA controller supports circular buffer

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management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to a dedicated hardware DMA request and can be triggered by using the software. The length, source, and destination of data to be transferred can be independently set by using the software. DMA can be used with the main peripherals, such as SPI, I2C, USART, TIMx, and ADC.

3.16 RTC

The real-time clock (RTC) has an independent binary-coded decimal (BCD) timer/counter. The RTC has the following features:

- Displays of the sub-seconds, seconds, minutes, hours (12- or 24-hour format), day of the week, day of the month, month, and year in BCD
- Automatic adjustment to the days of different months: 28 days, 29 days (leap year), 30 days, and 31 days
- A programmable alarm capable of wakeup from Stop and Standby mode
- Correction of 1 to 32,767 RTC clock pulses during runtime for synchronization between RTC and the main clock
- Digital calibration circuit with 1 ppm accuracy for compensation of deviation in crystal oscillators
- Two tamper detection pins with programmable filters. Wakeup from Stop or Standby mode when any tamper event is detected
- Timestamp feature used for the storage of calendar content. The timestamp feature can be triggered by the event on the timestamp pin or by the tamper event. MCUs can be woken up from Stop or Standby mode when any timestamp event is detected.
- Reference clock detection: a more accurate secondary clock source (50 Hz or 60 Hz) that can be used to improve calendar accuracy

3.17 IWDG

The independent watchdog (IWDG) is based on a 12-bit downcounter and an 8-bit prescaler. The IWDG is clocked by an internal independent 40 kHz RC oscillator. The RC oscillator is independent of the main clock, so it can operate in Stop mode and Standby mode. The IWDG can reset the system when a problem occurs, or work as a free-running timer that provides timeout management for applications. IWDG can be configured as a software or hardware watchdog through the option bytes. In debug mode, the counter can be frozen.

3.18 WWDG

The window watchdog (WWDG) is based on a 7-bit downcounter. The counter can be set to the free running mode or used as a watchdog to reset the system when a problem occurs. The WWDG is clocked by the system clock and has the early warning interrupt function. In debug mode, the counter can be frozen.

3.19 SysTick timer

SysTick timer is a dedicated timer of the operating system. It is a standard downcounter and has the following features:

- 24-bit downcounter
- Auto-reload capability
- Generates a maskable interrupt when the counter reaches 0
- Programmable clock source

3.20 Timers

Each HK32F030 MCU has an advanced timer, five general-purpose timers, and a basic timer. The following table describes the functions of each type of timer:

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Table 3-3 Functions of timers

Type	Timer	Counter Resolution	Counter Type	Prescaler Factor	DMA Request	Break Input	Capture/ Compare Channels	Complementary Outputs
Advanced	TIM1	16-bit	Up, down, up/down	Any integer from 1 to 65536	Yes	Yes	4	3
General-purpose	TIM3	16-bit	Up, down, up/down	Any integer from 1 to 65536	Yes	No	4	No
	TIM14	16-bit	Up, down, up/down	Any integer from 1 to 65536	No	No	1	No
	TIM15	16-bit	Up, down, up/down	Any integer from 1 to 65536	Yes	Yes	2	1
	TIM16	16-bit	Up, down, up/down	Any integer from 1 to 65536	Yes	Yes	1	1
	TIM17	16-bit	Up, down, up/down	Any integer from 1 to 65536	Yes	Yes	1	1
Basic	TIM6	16-bit	Up	Any integer from 1 to 65536	Yes	No	No	No

3.20.1 Basic timer

The basic timer TIM6 can be used as a generic 16-bit software time base.

3.20.2 General-purpose timer

Each general-purpose timer can be used to generate PWM outputs or serve as a simple time base.

- TIM3

  TIM3 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. It has four independent channels for input capture, output compare, PWM output, and one-pulse mode output.

  TIM3 can work with advanced timer TIM1 through the Timer Link feature for synchronization and event chaining. TIM3 can generate independent DMA requests. Additionally, TIM3 can handle quadrature (incremental) encoder signals and the digital outputs from one to three hall-effect sensors. In debug mode, the counter can be frozen.

- TIM14 and TIM15

  TIM14 and TIM15 are based on a 16-bit auto-reload up/down counter and a 16-bit prescaler respectively. TIM14 has one channel for input capture, output compare, PWM output, and one-pulse mode output. In debug mode, the counter can be frozen.

  TIM15 can generate DMA requests but TIM14 cannot.

- TIM16 and TIM17

  TIM16 and TIM17 are based on a 16-bit auto-reload up/down counter and a 16-bit prescaler respectively. They each have one channel for input capture, output compare, PWM output, and one-pulse mode output. TIM16 and TIM17 support complementary outputs with programmable inserted dead-times and can generate independent DMA requests. In debug mode, the counter can be frozen.

3.20.3 Advanced timer

The advanced timer TIM1 can be deemed as a three-phase PWM generator with six channels or used as a complete general-purpose timer. The four independent channels of TIM1 can be used for:

- Input capture
- Output compare

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- PWM generation (edge- or center-aligned mode)
- One-pulse mode output

Three of the four channels have complementary PWM outputs with programmable inserted dead-times.

If TIM1 is configured as a standard 16-bit timer, it has the same functions as TIMx. If TIM1 is configured as a 16-bit PWM generator, it has full modulation capability (0–100%). In debug mode, the counter can be frozen. Many functions of the advanced timer are the same as those of general-purpose timers, and the two types of timers have the same structure. Therefore, the advanced timer can work together with general-purpose timers through the Timer Link feature for synchronization or event chaining.

3.21 I2C bus

HK32F030 has two I2C bus interfaces. The I2C interface can work as a master or slave and supports the standard, fast, and fast mode plus (1 MHz) modes. The I2C interfaces support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). The I2C interfaces have embedded hardware CRC generation/verification. The I2C interfaces support SMBus 2.0 and PMBus 1.1: ARP capability, timeout verification, and ALERT protocol management.

Table 3-4 Programmable analog noise filter and digital noise filter

	Analog Filter	Digital Filter
Suppressed pulse width	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clock periods
Advantage	Available in Stop mode	1. Extra filtering capability, standard requirements 2. Stable length
Disadvantage	Performance changes along with the temperature, voltage, and process	-

3.22 USART

HK32F030 embeds two universal synchronous/asynchronous receivers/transmitters (USART1/USART2). The communication rate can be up to 9 Mbit/s. Both USART1 and USART2 provide management for CTS and RTS hardware flow control, RS485 DE signals, master synchronous communication, multiprocessor communication mode, and single-wire half-duplex communication mode. All USART interfaces can be served by the DMA controller.

The USARTs also support Smart Card communication (ISO 7816), IrDA SIR ENDEC, LIN master/slave capability, and automatic baud rate detection. The USARTs have a clock domain independent of the CPU clock, so they can wake up the MCU from Stop mode.

Table 3-5 USART features

USART Feature	USART1/USART2
Hardware flow control	Supported
Continuous communication via DMA	Supported
Multiprocessor communication	Supported
Synchronous mode	Supported
Smart Card mode	Supported
Single-wire half-duplex communication	Supported
IrDA SIR ENDEC	Supported
LIN mode	Supported
Dual clock domains and wakeup from Stop mode	Supported
Receiver timeout interrupt	Supported
Modbus communication	Supported
Automatic baud rate detection	Supported
Drive enable	Supported

3.23 SPI

HK32F030 has two serial peripheral interfaces (SPIs). In master or slave mode, the full-duplex and half-duplex communication speed is up to 18 Mbit/s. The 3-bit prescaler provides eight master mode frequencies. Each

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frame can be configured to 4-bit to 16-bit.

The standard I2S interfaces (with SPI multiplexed) provide four types of audio standards and can operate in master/slave half-duplex communication mode. The data format can be 16-bit, 24-bit, or 32-bit. The I2S interfaces can operate with 16- or 32-bit resolution and have dedicated signals for data synchronization. The I2S interfaces can be set to an audio sampling frequency from 8 kHz to 192 kHz by the 8-bit programmable linear prescaler. When working in master mode, the I2S interface can output a clock of 256 times the sampling frequency to external audio components.

Table 3-6 SPI features

SPI Feature	SPI1/SPI2
Hardware CRC calculation	Supported
Rx/Tx FIFO	Supported
NSS pulse mode	Supported
I2S mode	Supported
TI mode	Supported

3.24 GPIO

Each GPIO pin can be configured as an output pin (push-pull or open-drain), an input pin (floating, pull-up, or pull-down), or assigned to a peripheral alternate function by using the software. Most of the GPIO pins are shared by digital and analog peripherals. All GPIOs are high current-capable. I/O alternate functions can be locked as needed to prevent unexpected writes to the I/O registers.

3.25 ADC

HK32F030 has a 12-bit analog-to-digital converter (ADC) that can perform conversions in single or scan mode. In scan mode, the conversion is automatically performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface include:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single sample

The ADC can be served by the DMA controller. The analog watchdog feature provides precise voltage monitoring of one, some, or all selected channels. When the monitored voltage exceeds the preset threshold, an interrupt is generated. The events generated by general-purpose/advanced timers can be internally connected to the ADC start/injection trigger event respectively. The application program then synchronizes the A/D conversion and timers.

The ADC supports the sampling of 1/2 V_{DD}.

3.26 Temperature sensor

The temperature sensor generates a voltage that varies linearly based on the temperature. The temperature sensor is internally connected to the ADC1_IN16 input channel and is used to convert the sensor output voltage into a digital value.

3.27 Internal reference voltage

The internal reference voltage V_{REFINT} provides a stable voltage output for the ADC. V_{REFINT} is internally connected to the ADC_IN17 input channel and is read-only.

3.28 96-bit UID

The 96-bit unique identifier (UID) provides a reference number for each HK32F030 MCU. The UID is unique in any circumstances. You are not allowed to modify the UID. The 96-bit UID can be read in bytes (8 bits), half words (16 bits), or words (32 bits) for different applications. The 96-bit UID can be used:

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- As a serial number. For example, as a USB string serial number or used for other terminal applications.
- As a security key. When programming the Flash, use the UID together with software encryption and decryption algorithms to enhance the security of code in the Flash.
- To activate the boot processes that have the security mechanism.

3.29 Debug and trace port

Based on the ARM SWJ-DP embedded in HK32F030, SWDIO/SWCLK functions are available.

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4 Electrical characteristics

4.1 Absolute maximum values

The absolute maximum values are stress values within a short time.

Caution:

- Do not use the device in conditions equal to or exceeding the absolute maximum values.
- Stresses beyond the absolute maximum values listed in Table 4-1 to Table 4-3 may cause permanent damage to the device.
- If the device works under the maximum values for extended periods, its reliability may deteriorate.

4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD}–V_{SS}	External main power supply voltage (including V_{DDA} and V_{DD})	–0.5	6.0	V
V_{IN}	Input voltage on pins	–0.3	V_{DD} + 0.3	
$\lvert\Delta V_{DDx}\rvert$	Variation between different power pins	-	50	mV
$\lvert V_{SSx} - V_{SS}\rvert$	Variation between different ground pins	-	50	

4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} (source)(1)	150	mA
I_{VSS}	Total current from V_{SS} (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	–25	
$I_{INJ(PIN)}$(2)	Injected current on pins(3)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (all I/Os and control pins)(4)	±25	

(1). All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must be connected to the external power supply within the permitted range all the time.

(2). Negative injected current causes the analog performance of the device to fluctuate.

(3). When V_{IN} is larger than V_{DD}, a positive injected current is induced; when V_{IN} is smaller than V_{SS}, a negative injected current is induced. The injected current must be within the permitted range.

(4). If multiple I/Os have current injection simultaneously, the maximum $\sum I_{INJ(PIN)}$ is the sum of the absolute instantaneous values of the positive and negative injected currents.

4.1.3 Temperature characteristics

Table 4-3 Temperature characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	–45 to 150	°C
T_J	Maximum junction temperature	125	

4.2 Operating conditions

4.2.1 Recommended operating conditions

Table 4-4 Recommended operating conditions

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	0	72	
f_{PCLK2}	Internal APB2 clock frequency	0	72	
V_{DD}	Standard operating voltage	2	5.5	V
V_{DDA}(1)	Analog operating voltage	2	5.5	V
T	Operating temperature	–40	105	°C

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(1). V_{DDA} can be lower than V_{DD}. For example, if V_{DD} = 5 V, V_{DDA} = 3.3 V, or V_{DD} = 3.3 V, V_{DDA} = 2.5 V, the ADC can work normally.

4.2.2 PVD characteristics

Table 4-5 PVD characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (rising edge)	PLS[2:0] = 000	2.183	2.188	2.196	V
		PLS[2:0] = 001	2.286	2.289	2.298	
		PLS[2:0] = 010	2.393	2.399	2.407	
		PLS[2:0] = 011	2.502	2.508	2.518	
		PLS[2:0] = 100	2.621	2.629	2.639	
		PLS[2:0] = 101	2.726	2.733	2.745	
		PLS[2:0] = 110	2.839	2.846	2.855	
		PLS[2:0] = 111	2.958	2.969	2.979	
	Programmable voltage detector level selection (falling edge)	PLS[2:0] = 000	2.116	2.119	2.125	
		PLS[2:0] = 001	2.208	2.211	2.220	
		PLS[2:0] = 010	2.305	2.310	2.320	
		PLS[2:0] = 011	2.399	2.406	2.416	
		PLS[2:0] = 100	2.506	2.512	2.521	
		PLS[2:0] = 101	2.596	2.602	2.613	
		PLS[2:0] = 110	2.693	2.701	2.710	
		PLS[2:0] = 111	2.798	2.805	2.817	

4.2.3 Operating current characteristics

Table 4-6 Operating current characteristics

Mode	Condition	V_{DD}@25°C			Wakeup time@25°C@3.3 V	
		2.0 V	3.3 V	5.0 V	Wakeup code in Flash	Wakeup code in SRAM
Run	HCLK = 72 MHz, three wait states to access Flash, APB clock enabled	21.505 mA	22.63 mA	22.85 mA	-	-
	HCLK = 72 MHz, three wait states to access Flash, APB clock disabled	12.908 mA	13.232 mA	13.301 mA	-	-
	HCLK = HSE (8 MHz), zero wait states to access Flash, APB clock enabled	3.151 mA	3.418 mA	3.533 mA	-	-
	HCLK = HSE (8 MHz), zero wait states to access Flash, APB clock disabled	2.316 mA	2.559 mA	2.653 mA	-	-
	HCLK = LSI (40 kHz)	196 µA	208 µA	212 µA	-	-
	HCLK = LSE (32.768 kHz)	190 µA	205 µA	215 µA	-	-
Sleep	HCLK = 72 MHz, APB clock disabled	5.199 mA	5.441 mA	5.483 mA	575 ns	208 ns
	HCLK = HSI (8 MHz), APB clock disabled	0.778 mA	0.845 mA	0.937 mA	4.4 µs	1.55 µs
Stop	LDO operating at full speed, HSE/HSI/LSE disabled	126 µA	128 µA	130 µA	6.65 µs	6.6 µs
	LDO in low-power mode, HSE/HSI/LSE disabled	9.22 µA	10.26 µA	12.47 µA	19.4 µs	9.4 µs
Standby	LSI and LSE disabled	1.13 µA	1.64 µA	3.17 µA	172 µs	-
	RTC (LSI and IWDG enabled)	-	2.7 µA	-	172 µs	-
	RTC (LSE = 32.768 kHz)	-	2.6 µA	-	172 µs	-

4.2.4 Characteristics of external clocks

Table 4-7 HSE clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSE_ext}	Frequency	-	1	8	25	MHz
V_{HSEH}	High level voltage on the input pin		0.7V_{DD}	-	V_{DD}	V
V_{HSEL}	Low level voltage on the input pin		V_{SS}	-	0.3V_{DD}	
$T_{w(HSE)}$	Effective high/low level duration		5	-	-	ns
$T_{r(HSE)}$ $T_{f(HSE)}$	Rise/Fall time		-	-	20	
$Cin_{(HSE)}$	Input capacitance	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%

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Table 4-8 LSE clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{LSE_ext}	Frequency	-	-	32.768	1000	kHz
V_{LSEH}	High level voltage on the input pin		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	Low level voltage on the input pin		V_{SS}	-	$0.3V_{DD}$	
$Tw_{(LSE)}$	Effective high/low level duration		450	-	-	ns
$Tr_{(LSE)}$ $Tf_{(LSE)}$	Rise/Fall time		-	-	50	
$Cin_{(LSE)}$	Input capacitance	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%

4.2.5 Characteristics of internal clocks

Table 4-9 HSI clock characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	Oscillator accuracy	RCC_CR register calibrated		–1	-	1	
		Factory calibrated	T_A = –40°C to +105°C	–2	-	2.5	%
			T_A = –40°C to +85°C	–1.5	-	2.2	%
			T_A = 0°C to +70 °C	–1.3	-	2	%
			T_A = 25°C	–1.1	-	1.8	%
$T_{su(HSI)}$	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$		1	-	2	µs
$I_{DD(HSI)}$	Oscillator power consumption			-	80	100	µA

Table 4-10 LSI clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	30	40	60	kHz
$t_{su(LSI)}$	Oscillator startup time	-	-	-	85	µs
$I_{DD(LSI)}$	Oscillator power consumption			0.65	1.2	µA

4.2.6 PLL characteristics

Table 4-11 PLL characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{PLL_IN}	Input clock frequency	1	8.0	25	MHz
	Input clock duty cycle	40	-	60	%
f_{PLL_OUT}	Output clock frequency	16	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

4.2.7 Flash memory characteristics

Table 4-12 Flash memory characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{PROG}	Half word programming time	-	25	-	µs
	Word programming time	-	33	-	µs
T_{ERASE}	Half page erase time	-	9.2	-	ms
	Page erase time	-	4.6	-	ms
	Mass erase time	-	38	-	ms
IDD_{PROG}	Half byte programming current	-	-	5	mA
IDD_{ERASE}	Page/Mass erase current	-	-	2	mA
IDD_{READ}	Supply current@24 MHz (read mode)	-	2	3	mA
	Supply current@1 MHz (read mode)	-	0.25	0.4	mA
V_{IL}	Input low level voltage	-	-	$0.1 \times V_{DD}$	V
V_{IH}	Input high level voltage	$0.9 \times V_{DD}$	-	-	V
V_{OL}	Output low level voltage	-	-	$0.1 \times V_{DD}$	V
V_{OH}	Output high level voltage	$0.9 \times V_{DD}$	-	-	V
N_{END}	Erasure endurance	1	-	-	1k cycles
t_{RET}	Data retention	20	-	-	Years

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4.2.8 I/O pin characteristics

Table 4-13 I/O pin direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Symbol
V_{IH}	Input high level voltage	V_{DD} > 2 V	0.42 × (V_{DD} – 2 V) + 1 V		5.5	V
		V_{DD} ≤ 2 V			5.2	
V_{IL}	Input low level voltage		–0.3		0.32 × (V_{DD} – 2 V) + 0.75 V	V
V_{hys}	Schmitt trigger voltage hysteresis		5% × V_{DD}	-	-	mV
I_{lkg}	Input leakage current	V_{IN} = 5 V	-	-	3	μA
R_{PU}	Pull-up resistor	V_{IN} = V_{SS}	30	40	50	kΩ
R_{PD}	Pull-down resistor	V_{IN} = V_{DD}	30	40	50	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

Table 4-14 I/O pin alternating current characteristics

Mode OSPEEDy[1:0]	Symbol	Parameter	Condition	Min	Max	Unit
00/10	$f_{max(IO)out}$	Max frequency	C_L = 50 pF, V_{DD} = 2 V to 5.5 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	125	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125	
01	$f_{max(IO)out}$	Max frequency	C_L = 50 pF, V_{DD} = 2 V to 5.5 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	25	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25	
11	$f_{max(IO)out}$	Max frequency	C_L = 30 pF, V_{DD} = 2.7 V to 5.5 V	-	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 5.5 V	-	30	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	20	
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 5.5 V	-	5	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 5.5 V	-	8	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 5.5 V	-	5	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 5.5 V	-	8	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12	

4.2.9 TIM timer characteristics

Table 4-15 TIM characteristics

Symbol	Parameter	Min	Max	Unit
$T_{res(TIM)}$	Timer resolution time	1	-	$T_{TIM\ x\ CLK}$
F_{EXT}	Timer external clock frequency on CH1 to CH4	0	$F_{TIMxCLK}/2$ (1)	MHz
Res $_{TIM}$	Timer resolution	-	16	bit
$T_{counter}$	Clock period of the 16-bit counter when an internal clock is selected	1	65536	$T_{TIM\ x\ CLK}$
T_{MAX_COUNT}	Maximum possible count	-	65536 × 65536	$T_{TIM\ x\ CLK}$

(1). $f_{TIMxCLK}$ = 72 MHz

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4.2.10 ADC characteristics

Table 4-16 ADC characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog power supply voltage when ADC is enabled	-	2.0	3.3	5.5	V
INL	Integral non linearity (maximum difference between the actual conversion point and the end point correlation line)	f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, Test after calibration: V_{DDA} = 2.4 V to 3.6 V	–1.5	-	+1.5	LSB
DNL	Differential non linearity (maximum difference between the actual step and the ideal step)	f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, Test after calibration: V_{DDA} = 2.4 V to 3.6V	–1	-	+1	LSB
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S (1)	Sampling frequency	-	0.05		1	MHz
f_{TRIG} (1)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-		17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN} (1)	External input impedance	-	-	-	50	kΩ
R_{ADC} (1)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC} (1)	Sampling and hold capacitance	-	-	-	5	pF
t_{CAL} (1)	ADC calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	8.3			$1/f_{ADC}$
t_{latr} (1)	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2$ = 14 MHz	0.196			µs
		$f_{ADC} = f_{PCLK}/2$	5.5			$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4$ = 12 MHz	0.219			µs
		$f_{ADC} = f_{PCLK}/4$	10.5			$1/f_{PCLK}$
		$f_{ADC} = f_{HSI14}$ = 14 MHz	0.188	-	0.259	µs
$Jitter_{ADC}$	Jitters triggered by ADC conversions	$f_{ADC} = f_{HSI14}$	-	1	-	$1/f_{HSI14}$
t_S (1)	Sampling time	f_{ADC} = 14 MHz	0.107		17.1	µs
			1.5		239.5	$1/f_{ADC}$
t_{STAB} (1)	Sampling stable time	-	14			µs
t_{CONV} (1)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz, 12-bit resolution	1	-	18	µs
		12-bit resolution	14 to 252 (t_{CONV} = sampling time t_s + successive approximation time 12.5)			$1/f_{ADC}$

(1). The value is guaranteed in design but not tested in production.

4.2.11 Temperature sensor characteristics

Table 4-17 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Symbol
Sensor gain	-	-	3.92	-	mV/°C

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5 Pinouts and pin descriptions

HK32F030 MCUs are delivered in LQFP64, LQFP48, LQFP32, and TSSOP20 packages.

5.1 LQFP64

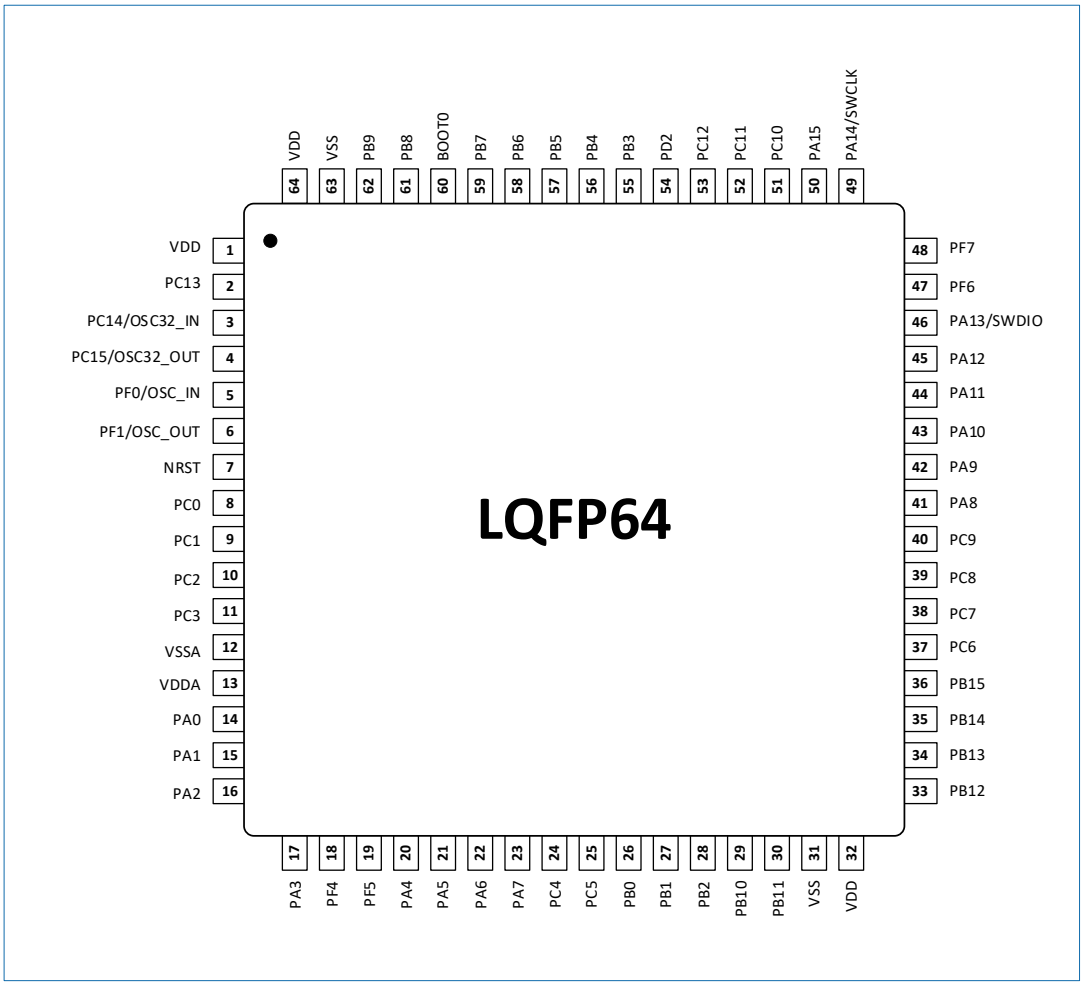

Figure 5-1 LQFP64 package pinout

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5.2 LQFP48

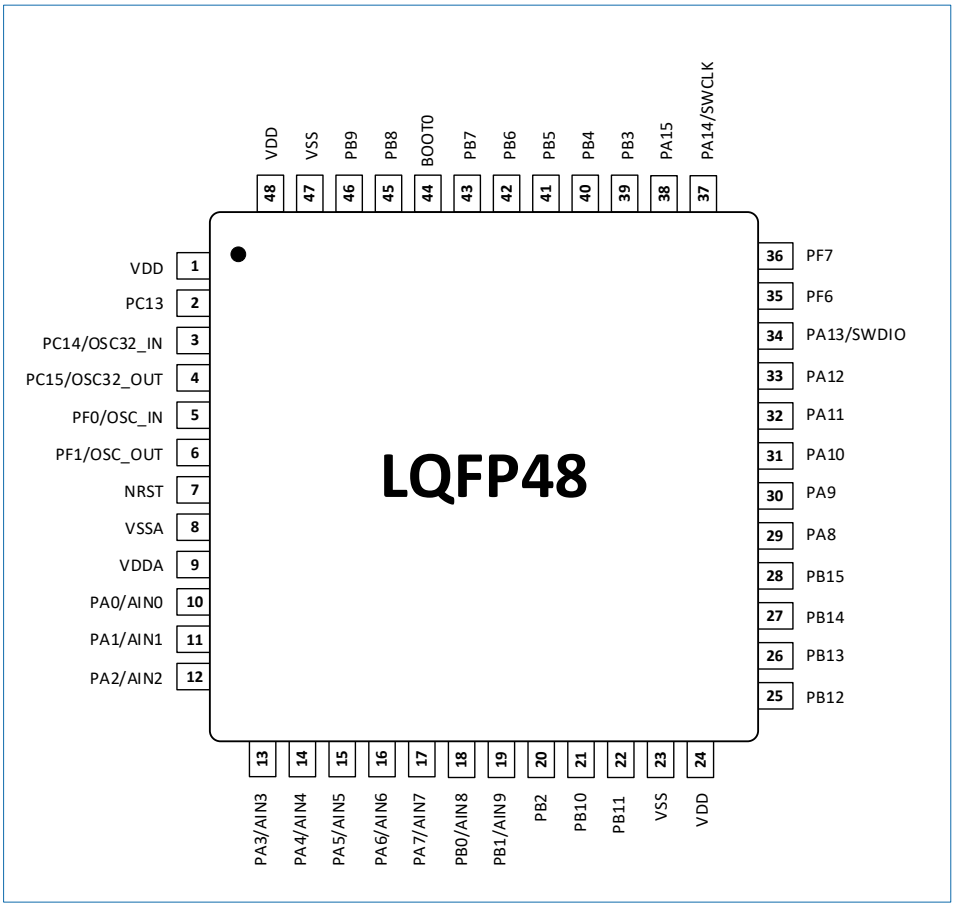

Figure 5-2 LQFP48 package pinout

5.3 LQFP32

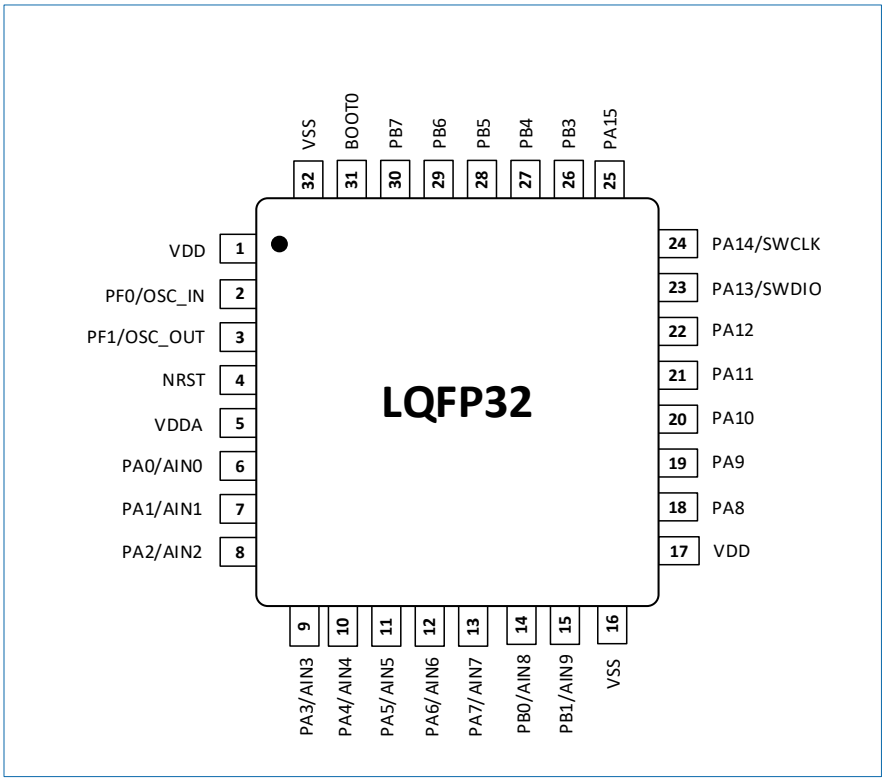

Figure 5-3 LQFP32 package pinout

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5.4 TSSOP20

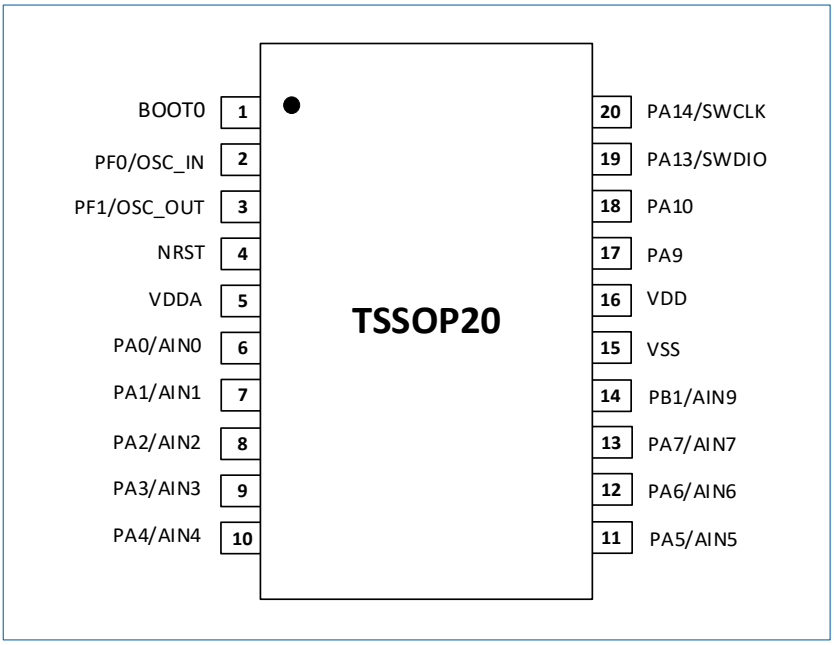

Figure 5-4 TSSOP20 package pinout

5.5 Pin descriptions

Table 5-1 Pin description of each package

LQFP64	LQFP48	LQFP32	TSSOP20	Name (Function after reset)	Type	Alternate Function	Additional Function
1	1	-	-	VDD	S (3)	Battery power supply input	
2	2	-	-	PC13	I/O	-	RTC_TAMP1 RTC_TS RTC_OUT WKUP2
3	3	-	-	PC14	I/O	-	OSC32_IN
4	4	-	-	PC15	I/O	-	OSC32_OUT
5	5	2	2	PF0	I/O	I2C1_SDA	OSC_IN
6	6	3	3	PF1	I/O	I2C1_SCL	OSC_OUT
7	7	4	4	NRST	I/O	Reset input/internal reset output, active low	
8	-	-	-	PC0	I/O	EVENTOUT	ADC_IN10 EXTI0
9	-	-	-	PC1	I/O	EVENTOUT	ADC_IN11 EXTI1
10	-	-	-	PC2	I/O	EVENTOUT SPI2_MISO I2S2_MCK	ADC_IN12 EXTI2
11	-	-	-	PC3	I/O	EVENTOUT SPI2_MOSI I2S2_SD	ADC_IN13 EXTI3
12	8	-	-	VSSA	S	Analog ground	
13	9	5	5	VDDA	S	Analog power supply	
14	10	6	6	PA0	I/O	USART1_CTS (1) USART2_CTS (2)	ADC_IN0 RTC_TAMP2 WKUP1 CKI_4 EXTI0
15	11	7	7	PA1	I/O	USART1_RTS (1) USART2_RTS (2) TIM15_CH1N EVENTOUT	ADC_IN1 EXTI1
16	12	8	8	PA2	I/O	USART1_TX (1) USART2_TX (2)	ADC_IN2 EXTI2

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LQFP64	LQFP48	LQFP32	TSSOP20	Name (Function after reset)	Type	Alternate Function	Additional Function
						USART1_RX (1) USART2_RX (2) TIM15_CH1	
17	13	9	9	PA3	I/O	USART1_RX (1) USART2_RX (2) USART1_TX (1) USART2_TX (2) TIM15_CH2	ADC_IN3 EXTI3
18	-	-	-	PF4	I/O	EVENTOUT	EXTI4
19	-	-	-	PF5	I/O	EVENTOUT	EXTI5
20	14	10	10	PA4	I/O	SPI1_NSS I2S1_WS USART1_CK (1) USART2_CK (2) TIM14_CH1	ADC_IN4 CKI_1 EXTI4
21	15	11	11	PA5	I/O	SPI1_SCK I2S1_CK	ADC_IN5 EXTI5
22	16	12	12	PA6	I/O	SPI1_MISO I2S1_MCK TIM3_CH1 TIM1_BKIN TIM16_CH1 EVENTOUT	ADC_IN6 EXTI6
23	17	13	13	PA7	I/O	SPI1_MOSI I2S1_SD TIM3_CH2 TIM14_CH1 TIM1_CH1N TIM17_CH1 EVENTOUT MCO	ADC_IN7 EXTI7
24	-	-	-	PC4	I/O	EVENTOUT	ADC_IN14 EXTI4
25	-	-	-	PC5	I/O	-	ADC_IN15 EXTI5
26	18	14	-	PB0	I/O	TIM3_CH3 TIM1_CH2N EVENTOUT	ADC_IN8 EXTI0
27	19	15	14	PB1	I/O	TIM3_CH4 TIM14_CH1 TIM1_CH3N	ADC_IN9 EXTI1
28	20	-	-	PB2	I/O	I2C1_SMBA (1) I2C2_SMBA (2)	EXTI2
29	21	-	-	PB10	I/O	I2C1_SCL (1) I2C2_SCL (2) SPI2_SCK I2S2_CK	EXTI10
30	22	-	-	PB11	I/O	I2C1_SDA (1) I2C2_SDA (2) EVENTOUT	EXTI11
31	23	16	15	VSS	I/O	Ground	
32	24	17	16	VDD	I/O	Digital power supply	
33	25	-	-	PB12	I/O	SPI1_NSS (1) I2S1_WS (1) SPI2_NSS (2) I2S2_WS (2) TIM1_BKIN TIM15_BKIN EVENTOUT I2C2_SMBA	EXTI12
34	26	-	-	PB13	I/O	SPI1_SCK (1) I2S1_CK (1) SPI2_SCK (2)	EXTI13

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LQFP64	LQFP48	LQFP32	TSSOP20	Name (Function after reset)	Type	Alternate Function	Additional Function
						I2S2_CK(2) TIM1_CH1N I2C2_SCL	
35	27	-	-	PB14	I/O	SPI1_MISO (1) I2S1_MCK (1) SPI2_MISO (2) I2S2_MCK(2) TIM1_CH2N TIM15_CH1 I2C2_SDA	EXTI14
36	28	-	-	PB15	I/O	SPI1_MOSI (1) I2S1_SD (1) SPI2_MOSI (2) I2S2_SD (2) TIM1_CH3N TIM15_CH1N TIM15_CH2	RTC_REFIN EXTI15
37	-	-	-	PC6	I/O	TIM3_CH1	EXTI6
38	-	-	-	PC7	I/O	TIM3_CH2	EXTI7
39	-	-	-	PC8	I/O	TIM3_CH3	EXTI8
40	-	-	-	PC9	I/O	TIM3_CH4	EXTI9
41	29	18	-	PA8	I/O	USART1_CK TIM1_CH1 EVENTOUT MCO	EXTI8
42	30	19	17	PA9	I/O	USART1_TX (1) USART1_RX (1) TIM1_CH2 TIM15_BKIN I2C1_SCL MCO	EXTI9
43	31	20	18	PA10	I/O	USART1_RX (1) USART1_TX (1) TIM1_CH3 TIM17_BKIN I2C1_SDA	EXTI10
44	32	21	-	PA11	I/O	USART1_CTS TIM1_CH4 EVENTOUT I2C2_SCL	EXTI11
45	33	22	-	PA12	I/O	USART1_RTS TIM1_ETR EVENTOUT I2C2_SDA	EXTI12
46	34	23	19	PA13	I/O	IRTIM_OUT SWDIO	CKI_2 EXTI13
47	35	-	-	PF6	I/O	I2C1_SCL(1) I2C2_SCL (2)	EXTI6
48	36	-	-	PF7	I/O	I2C1_SDA(1) I2C2_SDA (2)	EXTI7
49	37	24	20	PA14	I/O	USART1_TX (1) USART1_RX (1) USART2_TX (2) USART2_RX (2) SWCLK	CKI_3 EXTI14
50	38	25	-	PA15	I/O	SPI1_NSS I2S1_WS USART1_RX(1) USART1_TX(1) USART2_RX(2) USART2_TX(2) EVENTOUT	EXTI15
51	-	-	-	PC10	I/O	-	EXTI10

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LQFP64	LQFP48	LQFP32	TSSOP20	Name (Function after reset)	Type	Alternate Function	Additional Function
52	-	-	-	PC11	I/O	-	EXTI11
53	-	-	-	PC12	I/O	-	EXTI12
54	-	-	-	PD2	I/O	TIM3_ETR	EXTI2
55	39	26	-	PB3	I/O	SPI1_SCK I2S1_CK EVENTOUT	EXTI3
56	40	27	-	PB4	I/O	SPI1_MISO I2S1_MCK TIM3_CH1 EVENTOUT TIM17_BKIN	EXTI4
57	41	28	-	PB5	I/O	SPI1_MOSI I2S1_SD I2C1_SMBA TIM16_BKIN TIM3_CH2	EXTI5
58	42	29	-	PB6	I/O	I2C1_SCL USART1_TX USART1_RX TIM16_CH1N	EXTI6
59	43	30	-	PB7	I/O	I2C1_SDA USART1_RX USART1_TX TIM17_CH1N	EXTI7
60	44	31	1	Boot0(4)	I	Boot memory selection	
61	45	-	-	PB8	I/O	I2C1_SCL TIM16_CH1	EXTI8
62	46	-	-	PB9	I/O	I2C1_SDA IRTIM_OUT TIM17_CH1 EVENTOUT SPI2_NSS I2S2_WS	EXTI9
63	47	32	15	VSS	S	Ground	
64	48	1	16	VDD	S	Digital power supply	

(1). This function is only available in HK32F030x4 and HK32F030x6.

(2). This function is only available in HK32F030x8.

(3). I = input, O = output, I/O = input/output, S = power supply.

5.6 GPIO alternate function tables

Table 5-2 Alternate function table of GPIO Port A

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF15
PA0	-	USART1_CTS (1)/ USART2_CTS (2)	-	-	-	-	-	-
PA1	EVENTOUT	USART1_RTS (1)/ USART2_RTS (2)	-	-	-	TIM15_CH1N	-	-
PA2	TIM15_CH1	USART1_TX (1)/ USART1_RX (1)(3)	-	-	-	-	-	-
		USART2_TX (2)/ USART2_RX (2) (3)						
PA3	TIM15_CH2	USART1_RX (1)/ USART1_TX (1) (3)	-	-	-	-	-	-
		USART2_RX (2)/ USART2_TX (2) (3)						
PA4	SPI1_NSS I2S1_WS	USART1_CK (1) USART2_CK (2)	-	-	TIM14_CH1	-	-	-
PA5	SPI1_SCK	-	-	-		-	-	-

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF15
	I2S1_CK							
PA6	SPI1_MISO I2S1_MCK	TIM3_CH1	TIM1_BKIN	-	-	TIM16_CH1	EVENTOUT	-
PA7	SPI1_MOSI I2S1_SD	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT	MCO
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	-	-	-	-
PA9	TIM15_BKIN	USART1_TX/ USART1_RX(3)	TIM1_CH2	-	I2C1_SCL	MCO	-	-
PA10	TIM17_BKIN	USART1_RX/ USART1_TX(3)	TIM1_CH3	-	I2C1_SDA	-	-	-
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	-	-	I2C2_SCL	-	-
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	-	-	I2C2_SDA	-	-
PA13	SWDIO	IRTIM_OUT	-	-	-	-	-	-
PA14	SWCLK	USART1_TX (1)/ USART1_RX (1) (3)	-	-	-	-	-	-
		USART2_TX (2)/ USART2_RX (2) (3)						
PA15	SPI1_NSS I2S1_WS	USART1_RX (1)/ USART1_TX (1) (3)	-	EVENTOUT	-	-	-	-
		USART2_RX (2)/ USART2_TX (2) (3)						

(1). This function is only available in HK32F030x4 and HK32F030x6.

(2). This function is only available in HK32F030x8.

(3). When USART_CTRL2.SWAP = 1, the functions of USART_TX and USART_RX pins in the same USART group are exchanged. For example, USART1_TX and USART1_RX can be exchanged.

Table 5-3 Alternate function table of GPIO Port B

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF15
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	-	-	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	-	-	-	-
PB2	-	-	-	-	-	-	-	I2C1_SMBA (2)/ I2C2_SMBA (3)
PB3	SPI1_SCK I2S1_CK	EVENTOUT	-	-	-	-	-	-
PB4	SPI1_MISO I2S1_MCK	TIM3_CH1	EVENTOUT	-	-	TIM17_BKIN	-	-
PB5	SPI1_MOSI I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	-	-	-	-
PB6	USART1_TX/ USART1_RX(1)	I2C1_SCL	TIM16_CH1N	-	-	-	-	-
PB7	USART1_RX/ USART1_TX(1)	I2C1_SDA	TIM17_CH1N	-	-	-	-	-
PB8	-	I2C1_SCL	TIM16_CH1	-	-	-	-	-
PB9	IRTIM_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT	-	SPI2_NSS I2S2_WS	-	-
PB10	-	I2C1_SCL(2)/ I2C2_SCL (3)	-	-	-	SPI2_SCK I2S2_CK	-	-
PB11	EVENTOUT	I2C1_SDA(2)/ I2C2_SDA (3)	-	-	-	-	-	-
PB12	SPI1_NSS (2) / I2S1_WS (2)	EVENTOUT	TIM1_BKIN	-	-	TIM15_BKIN	-	I2C2_SMBA
	SPI2_NSS (3)/ I2S2_WS (3)							
PB13	SPI1_SCK (2)/ I2S1_CK (2)	-	TIM1_CH1N	-	-	I2C2_SCL	-	-
	SPI2_SCK (3)/ I2S2_CK (3)							
PB14	SPI1_MISO(2)/ I2S1_MCK (2)	TIM15_CH1	TIM1_CH2N	-	-	I2C2_SDA	-	-

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Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF15
	SPI2_MISO [3]/ I2S2_MCK [3]							
PB15	SPI1_MOSI[2]/ I2S1_SD[2]	TIM15_CH2	TIM1_CH3N	TIM15_CH1N	-	-	-	-
	SPI2_MOSI [3]/ I2S2_SD [3]							

(1). When USART_CTRL2.SWAP = 1, the functions of USART_TX and USART_RX pins in the same USART group are exchanged.

(2). This function is only available in HK32F030x4 and HK32F030x6.

(3). This function is only available in HK32F030x8.

Table 5-4 Alternate function table of GPIO Port C

Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	EVENTOUT	-	-	-	-	-	-	-
PC1	EVENTOUT	-	-	-	-	-	-	-
PC2	EVENTOUT	SPI2_MISO/I2S2_MCK	-	-	-	-	-	-
PC3	EVENTOUT	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-
PC4	EVENTOUT	-	-	-	-	-	-	-
PC5	-	-	-	-	-	-	-	-
PC6	TIM3_CH1	-	-	-	-	-	-	-
PC7	TIM3_CH2	-	-	-	-	-	-	-
PC8	TIM3_CH3	-	-	-	-	-	-	-
PC9	TIM3_CH4	-	-	-	-	-	-	-
PC10	-	-	-	-	-	-	-	-
PC11	-	-	-	-	-	-	-	-
PC12	-	-	-	-	-	-	-	-
PC13	-	-	-	-	-	-	-	-
PC14	-	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-	-

Table 5-5 Alternate function table of GPIO Port D

Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD2	TIM3_ETR	-	-	-	-	-	-	-

Table 5-6 Alternate function table of GPIO Port F

Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	-	I2C1_SDA	-	-	-	-	-	-
PF1	-	I2C1_SCL	-	-	-	-	-	-
PF4	EVENTOUT	-	-	-	-	-	-	-
PF5	EVENTOUT	-	-	-	-	-	-	-
PF6	-	I2C1_SCL(1) I2C2_SCL(2)	-	-	-	-	-	-
PF7	-	I2C1_SDA(1) I2C2_SDA(2)	-	-	-	-	-	-

(1). This function is only available in HK32F030x4 and HK32F030x6.

(2). This function is only available in HK32F030x8.

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6 Packages

6.1 Package outlines

6.1.1 LQFP64

LQFP64 is a 10 mm × 10 mm, 0.5 mm pitch, 64-pin low-profile quad flat package.

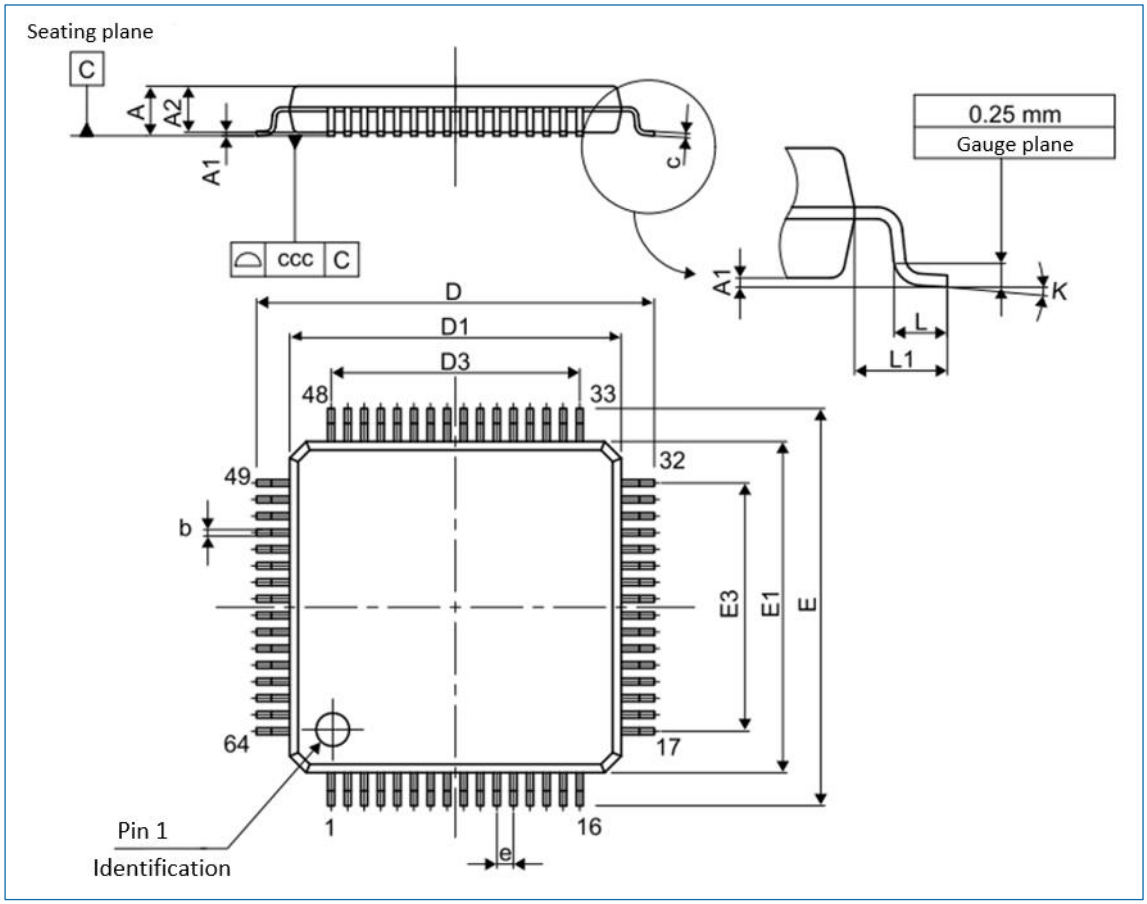

Figure 6-1 LQFP64 package outline

Table 6-1 LQFP64 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)	Min (inches) (1)	Typ (inches)(1)	Max (inches)(1)
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

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6.1.2 LQFP48

LQFP48 is a 7 mm × 7 mm, 0.5 mm pitch, 48-pin low-profile quad flat package.

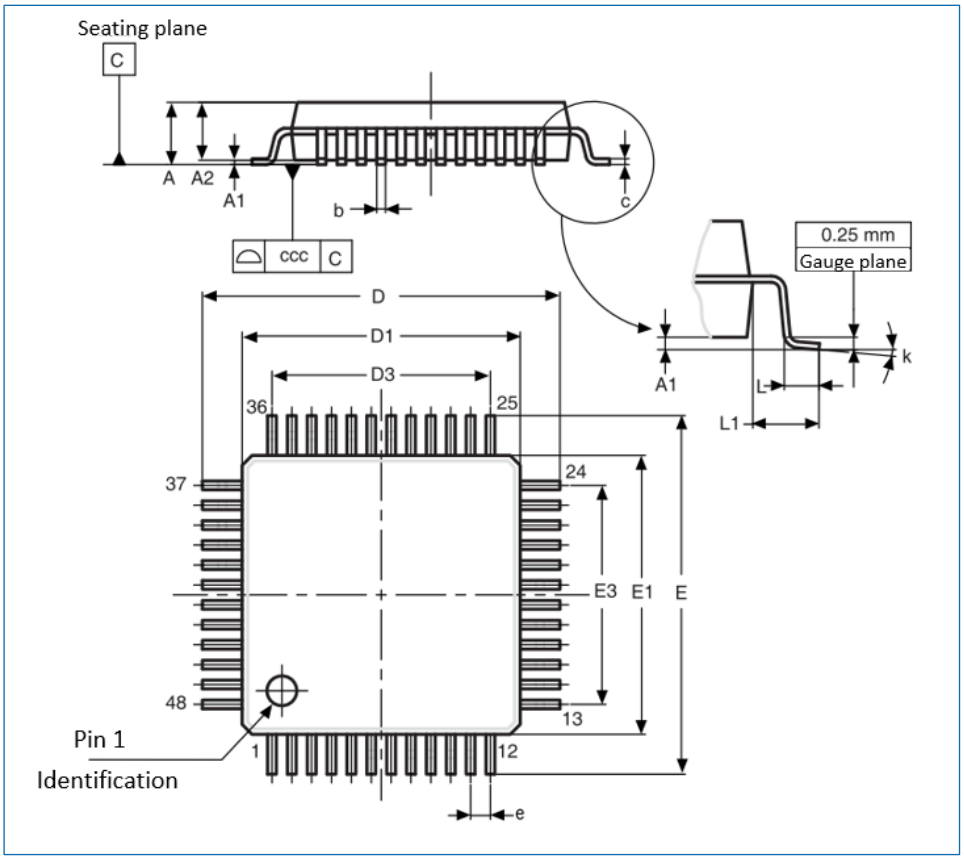

Figure 6-2 LQFP48 package outline

Table 6-2 LQFP48 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)	Min (inches)(1)	Typ (inches)(1)	Max (inches)(1)
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

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6.1.3 LQFP32

LQFP32 is a 7 mm × 7 mm, 0.8 mm pitch, 32-pin low-profile quad flat package.

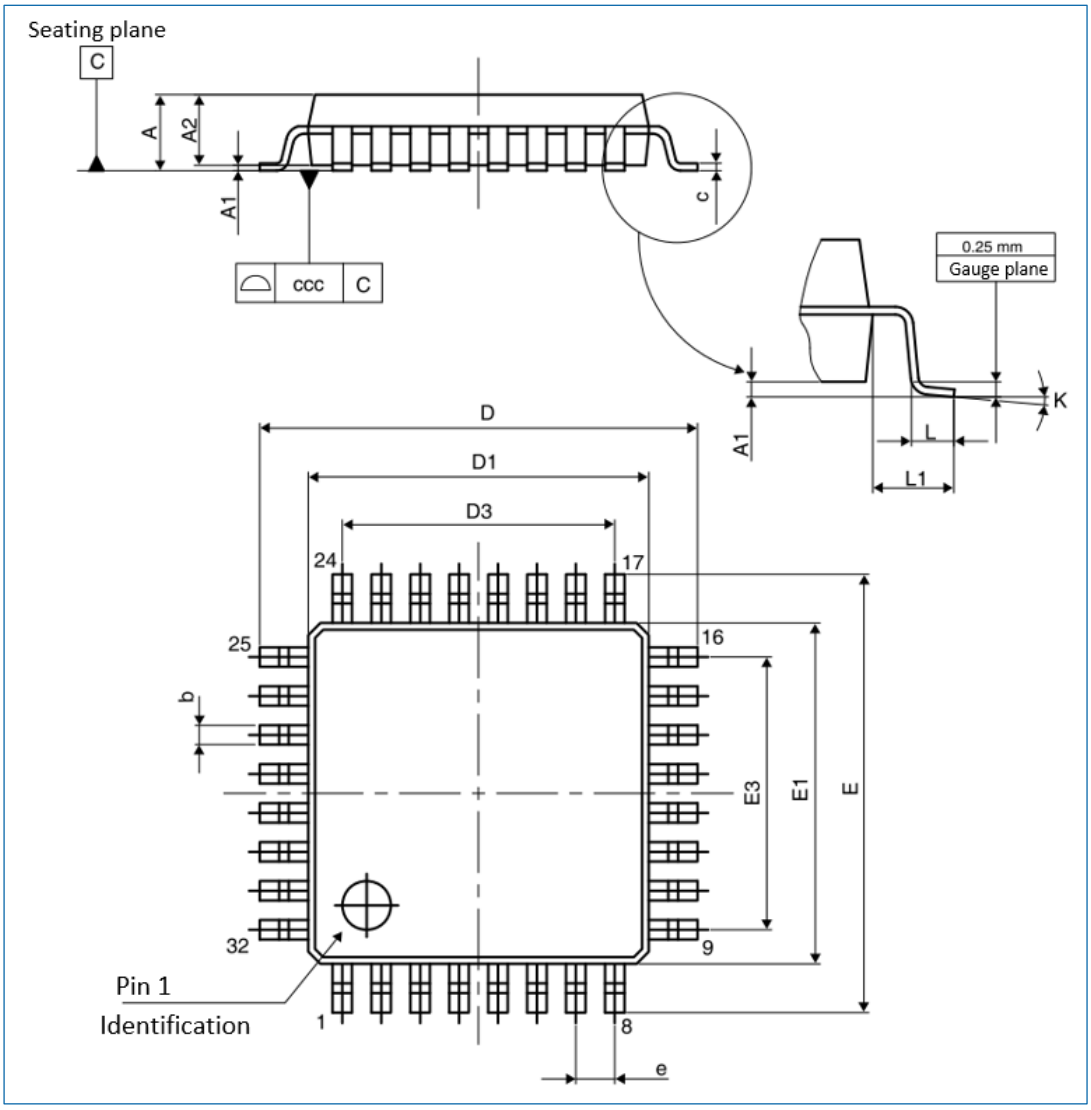

Figure 6-3 LQFP32 package outline

Table 6-3 LQFP32 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)	Min (inches)(1)	Typ (inches)(1)	Max (inches)(1)
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

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6.1.4 TSSOP20

TSSOP20 is a 6.5 mm x 4.4 mm, 0.65 mm pitch package.

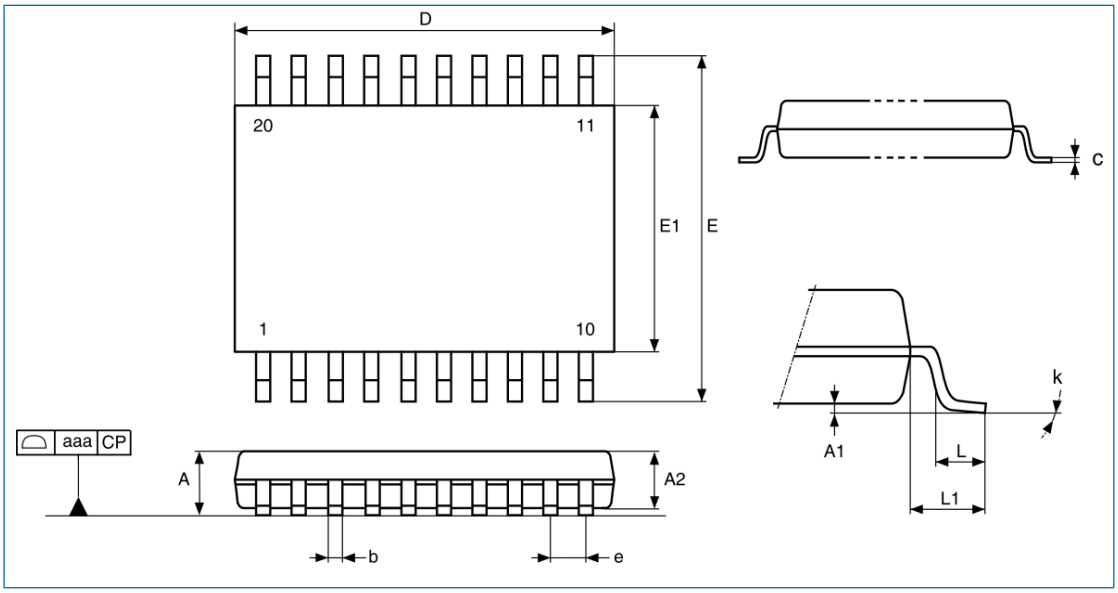

Figure 6-4 TSSOP20 package outline

Table 6-4 TSSOP20 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)	Min (inches)(1)	Typ (inches)(1)	Max (inches)(1)
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190		0.300	0.0075		0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°		8.0°	0°		8.0°
ccc	-	-	0.100	-	-	0.0039

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

6.2 Device marking

The device marking consists of the Hangshun logo, ARM logo, part number, and lot number. The following table describes the lot number:

Table 6-5 Lot number description

Lot Number	Description
First character	The year when the MCU was manufactured. For example, 1 indicates the year 2021.
Second and third characters	The assembly factory.
Fourth and fifth characters	The week in which the order was placed. For example, 18 indicates that the order was placed in the 18th week of the year.
Sixth, seventh, and eighth characters	The last three characters of the wafer lot number.

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6.2.1 LQFP64 marking

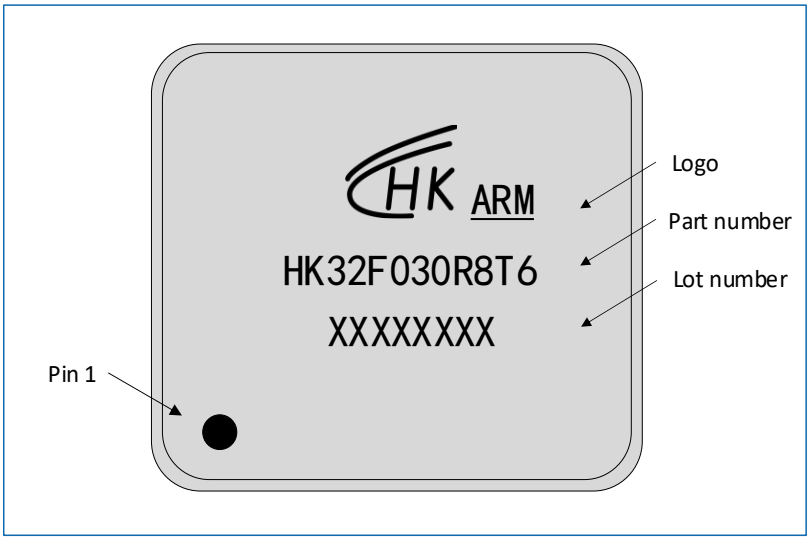

Figure 6-5 LQFP64 HK32F030R8T6 marking example

6.2.2 LQFP48 marking

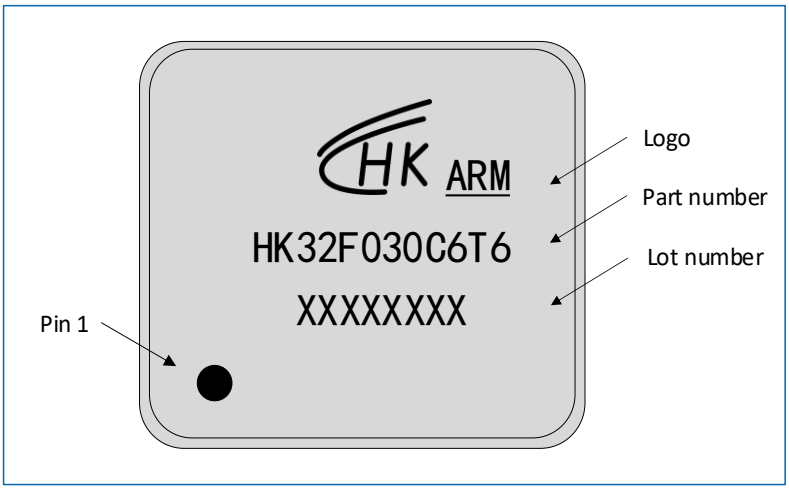

Figure 6-6 LQFP48 HK32F030C6T6 marking example

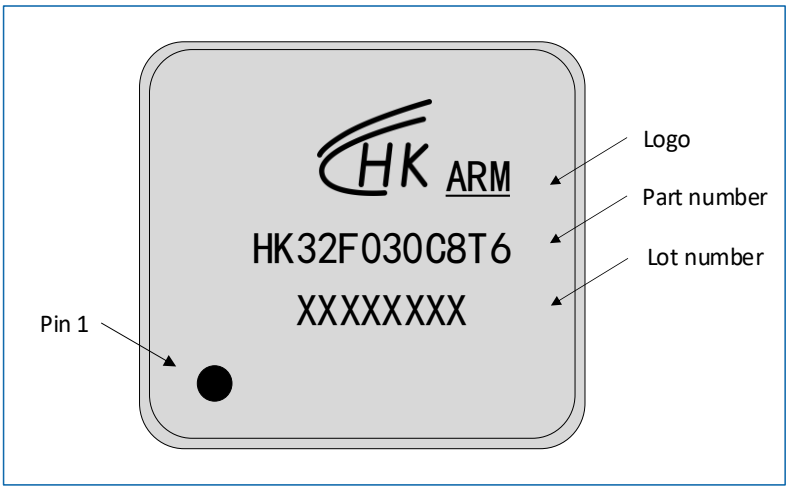

Figure 6-7 LQFP48 HK32F030C8T6 marking example

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6.2.3 LQFP32 marking

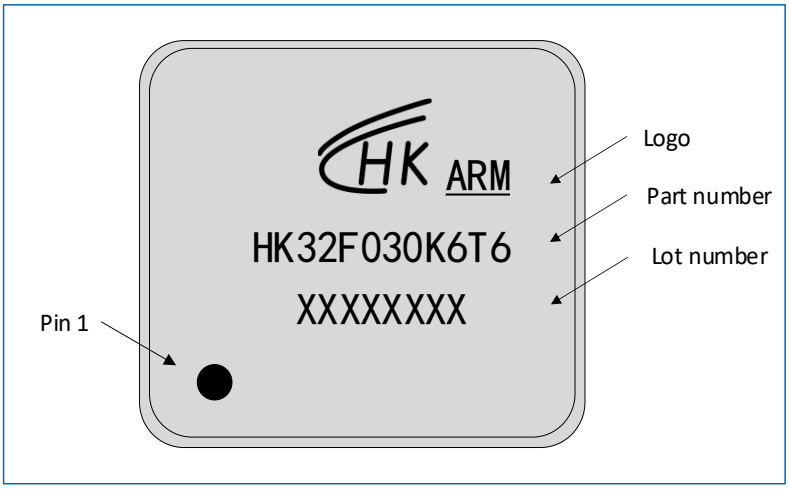

Figure 6-8 LQFP32 HK32F030K6T6 marking example

6.2.4 TSSOP20 marking

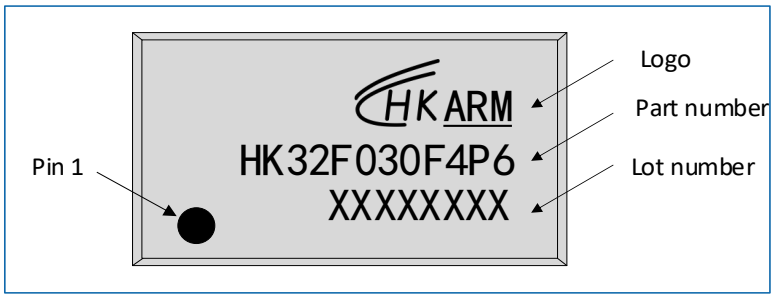

Figure 6-9 TSSOP20 HK32F030F4P6 marking example

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7 Ordering information

7.1 Device numbering conventions

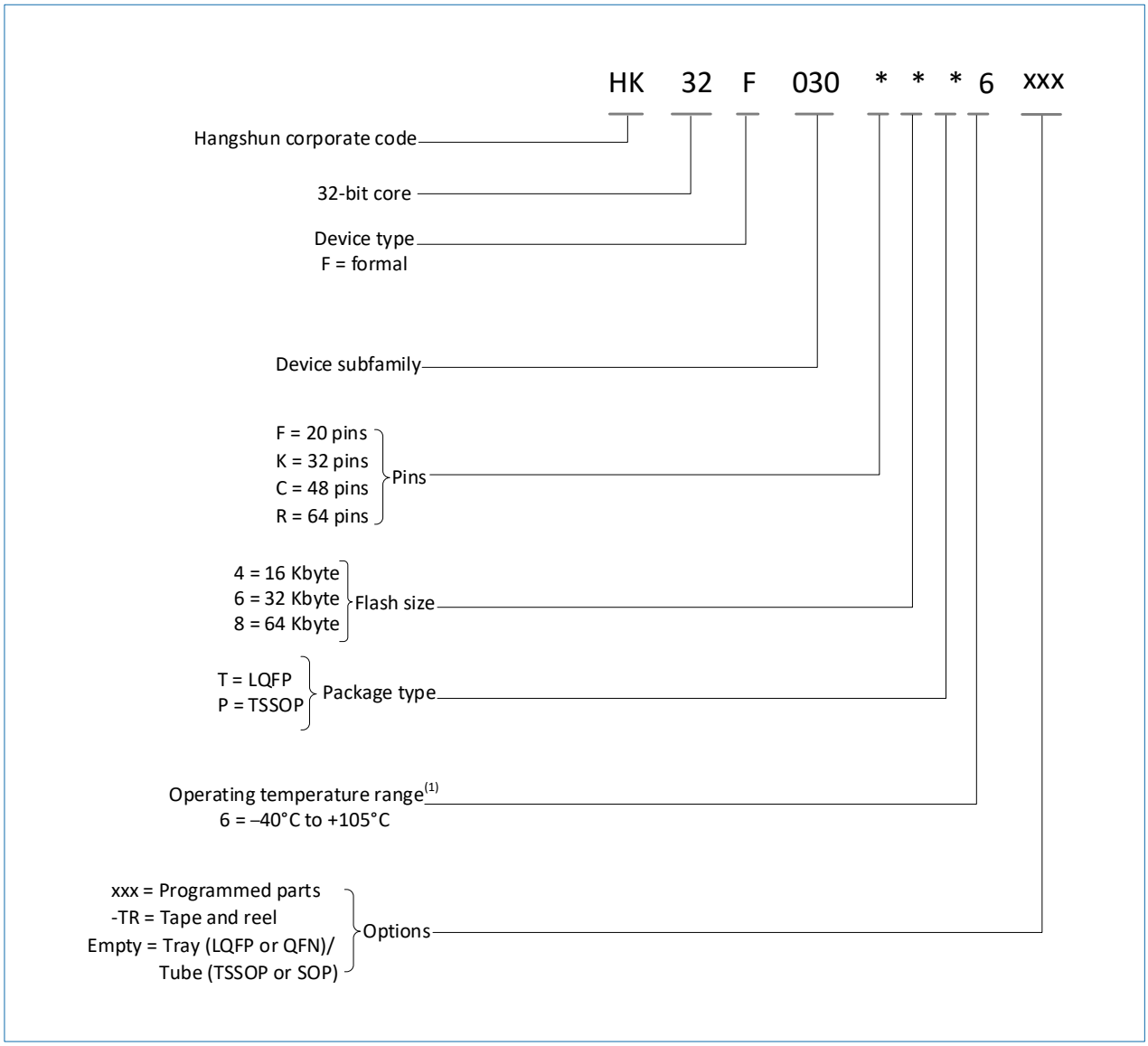

Figure 7-1 Device numbering conventions

Note:

The HK32F030 series was first released in earlier times, so its device numbering is based on *Hangshun Product Naming Conventions V0.9,* which is slightly different from the latest naming conventions.

7.2 Packaging information

Table 7-1 HK32F030 packaging information

Package	Part Number	Shipping Option	Remarks
LQFP64	HK32F030R8T6	Tray	
LQFP64	HK32F030R8T6-TR	Tape and reel	
LQFP48	HK32F030C6T6	Tray	
LQFP48	HK32F030C6T6-TR	Tape and reel	
LQFP48	HK32F030C8T6	Tray	
LQFP48	HK32F030C8T6-TR	Tape and reel	
LQFP32	HK32F030K6T6	Tray	
LQFP32	HK32F030K6T6-TR	Tape and reel	
TSSOP20	HK32F030F4P6	Tube	
TSSOP20	HK32F030F4P6-TR	Tape and reel	

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8 Acronyms

Term	Full Name
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CAN	Controller Area Network
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
EXTI	Extended Interrupt/Event Controller
FM	Fast Mode
GPIO	General-purpose Input/Output
HSE	High-speed External (clock signal)
I2C	Inter-integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSB	Least Significant Bit
LSE	Low-Speed External (clock signal)
LSI	Low-speed Internal (clock signal)
MCU	Microcontroller Unit
MSB	Most Significant Bit
MSPS	Million Samples Per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-down Reset
PLL	Phase-locked Loop
POR	Power-on Reset
PVD	Programmable Voltage Detector
PWM	Pulse Width Modulation
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computer
RTC	Real-time Clock
SDIO	Secure Digital Input and Output
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
WWDG	Window Watchdog

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